Final Technical Report

Novel SiC High Power IC Technology

Supported under Grant # N00014-98-1-0534
Office of the Chief of Naval Research
Report for the period 4/1/98 - 6/20/01

B.J. Baliga, P. R. Singh, S. Sonkusale, A. Venkateswaran,
P. Mehrotra, S. Harney , S. Venkatesan
Department of Electrical and Computer Engineering,
North Carolina State University,
Campus Box 7924,
Raleigh, NC 27695-7924

June, 2001

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY (*Leave Blank*)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	June 20, 2001	Final Technical Report (April 1, 1998 through June 20, 2001)

4. TITLE AND SUBTITLE
Novel SiC High Power IC Technology
High Voltage 4H-SiC Lateral RESURF Devices
Silicon Carbide High voltage Lateral RESURF MOSFETs and RESURF Diodes.
A Novel Device Isolation Technology for 4H- SiC

5. FUNDING NUMBERS
PR Number 98PR05288-00

6. AUTHORS
B. J. Baliga, P. Mehrotra, A. Venkateswaran, S. Sonkusale, P. R. Singh, S. Venkatesan
S. Harney

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
North Carolina State University
Hillsborough Street
Raleigh, NC 27695

8. PERFORMING ORGANIZATION REPORT NUMBER
N00014-98-1-0534

9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Sponsoring: ONR, Code 254: North Quincy Street, Arlington, VA 22217-5660
Monitoring: administrative Grants Officer, ONR Regional Office Atlanta
Regional Office, Suite 4R15, 100 alabama Street NW
Atlanta, GA 30303-3104

10. SPONSORING / MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES

12a. DISTRIBUTION / AVAILABILITY STATEMENT
Approved for Public Release; Distribution Unlimited

12b. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 words)*

The devices used in the military need to be operated at high voltage ,high temperature and high frequency .Silicon Carbide is an attractive material for the development of such devices. SiC has the critical field ten times higher than that of the silicon . This implies that lateral RESURF devices made in SIC can support the same breakdown voltage in a much smaller drift length as compared to the silicon devices. In our project we are using the concept of Lateral RESURF device to obtain diodes and MOSFETs having high breakdown and small specific on-resistance From the results of two dimensional numerical simulations on the RESURF devices ,it was found that in RESURF diodes high breakdown voltage (>2000 V) is possible for the RESURF dose of up to 2×10^{13} cm^{-2} ,which is 10-20 times higher than for silicon devices. Also in LATERAL RESURF MOSFETs high breakdown voltage (>1800)was possible for RESURF dose of up to 1×10^{13} cm^{-2} ,which is 5-10 times higher than for silicon MOSFETs. The specific on resistance of these devices was found to be less than 100 mohm- cm^2.

The vertical channel structure is more suitable for a power device because of higher device density and because of reduction in the electric field crowding in the device. At the same time lateral devices offer simplicity in fabrication. To optimize a Power IC, it will be good to have both, vertical and lateral devices. The vertical isolation layer is formed by creating deep level traps through ion implantation of light neutral ions, such as hydrogen and helium. It is demonstrated that the 4H-SiC lateral N-channel MOSFETs and P-channel MOSFETs can be fabricated in the thin active SiC layer formed on top of a high resistivity isolation layer.

14. SUBJECT TERMS
RESURF, Gauss's Law, Silicon Carbide, Oxide Rupture Filed, Dielectric Constant, Electric Field Profile, Nitride MOSFETs, Diode, N-Channel, P-Channel, Isolation layer, Lateral.

15. NUMBER OF PAGES
35

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
Unclassified	Unclassified	Unclassified	SAR

Table of Content

4H SiC Lateral Single Zone RESURF Diodes.

Pronita Mehrotra, B. Jayant Baliga
Power semiconductor Research Center
North Carolina State University
Raleigh, NC 27606

Abstract

The combination of the electronic and the physical properties of the silicon carbide (SiC) make it an excellent semiconductor for the electronic devices capable of working in hostile environments where conventional semiconductors like Si and GaAs cannot perform operations. The critical electric field of SiC is one order higher than that of Si, which allows much higher doping and thinner drift region layer for a given blocking voltage , resulting in a lower specific on-resistance. This implies that lateral RESURF (REduced SURface Field) devices made in SiC can support the same breakdown voltage in a much smaller drift length, as compared to silicon devices. Extensive work has been done in SiC , a more comprehensive analysis still remains to be done. The goal of the rest of the report is to show simulation results for the RESURF diodes in SiC.

4H SiC Lateral Single Zone RESURF Diodes

Pronita Mehrotra, B. Jayant Baliga
Power Semiconductor Research Center
North Carolina State University
Raleigh, NC 27606

Introduction

Silicon Carbide is an attractive material for development of high voltage, high temperature and high frequency devices. The critical electric field of Silicon Carbide is more than 10 times higher than that of Silicon. This implies that lateral RESURF (REduced SURface Field) devices made in SiC can support the same breakdown voltage in a much smaller drift length, as compared to silicon devices [1]. Extensive work has been done on RESURF devices in Si [2-4], and though some work has been done in SiC [5], a more comprehensive analysis still remains to be done. The goal of the rest of the report is to show simulation results for RESURF diodes in SiC. The breakdown of a RESURF device depends on the RESURF layer dose and the RESURF layer length. From Si studies it is known that the breakdown voltage is low for very high and very low doses and is high for intermediate doses and that it increases linearly with the RESURF length till it reaches a maximum value limited by breakdown at the epi-substrate junction. Therefore, the RESURF layer has to be optimized for dose and length to achieve high breakdown voltages in SiC devices. In this work, the optimization was performed for the 4-H polytype.

Device Structure 1

Fig. 1 shows the cross-section of a lateral single zone RESURF diode. The basic structure consists of two p-n junctions: a vertical P^+N_{res} junction and a horizontal P^-N_{res} junction. Considering these parts as one-dimensional junctions, the vertical junction has a lower breakdown voltage compared to the horizontal junction. The doping of the P^-epi layer determines the voltage that can be supported by the device when breakdown occurs at the horizontal junction shown in Fig.1.

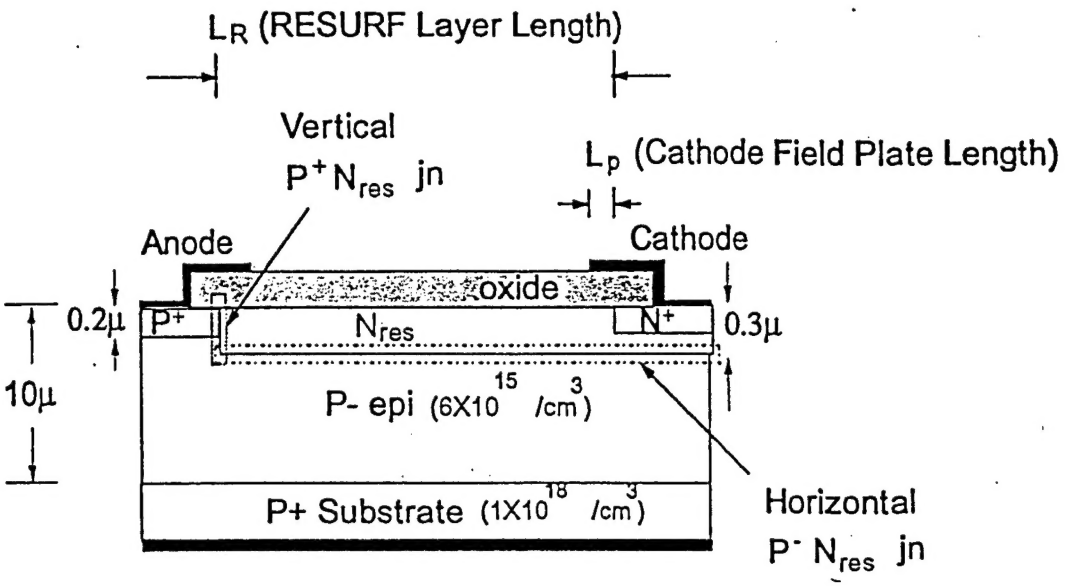


Fig 1 Cross-section of a single zone lateral SiC RESURF diode

Due to the RESURF action, the depletion of the vertical P^+N_{res} junction is reinforced by the horizontal junction. Consequently, for the same applied voltage, the depletion stretches along the surface over a much longer distance than would be expected according to simple one-dimensional calculations. As a result, the electric field at the surface is reduced and surface breakdown can be eliminated [6] The total charge in the drift region needs to be adjusted to an optimum value in accordance with the RESURF principle to achieve maximum possible breakdown voltage. Therefore, simulations were carried out for various RESURF layer doses and for different RESURF lengths. These simulation results are discussed next.

Simulation Results

To start with a 1 dimensional simulation was done, on the device simulator, MEDICI, to determine the ideal parallel plane breakdown voltage of vertical $N^+N_{res}P^-P^+$ diode formed at the cathode end as seen from Fig. 1. The epi-layer thickness, RESURF layer thickness and the dopings are as shown in Fig. 1 This is the maximum breakdown voltage that we can expect for our device. From the 1D simulations, the breakdown voltage was found to be 2380V. Also for the optimum case, the RESURF layer has to be fully depleted when the electric field reaches the critical electric field for breakdown at the horizontal p-n junction. Assuming a uniform electric field profile in the RESURF layer, using Gauss's law, we get the optimum charge to be

$$Q = (qN_Dt) = \varepsilon_s E_c \qquad (1)$$

where N_D is the doping of the RESURF layer, t is the thickness of the layer, ε_s is the permittivity of SiC and E_c is the critical electric field in SiC. The critical electric field is hard to determine for our structure, but as an approximation we took E_c the same as that for a n^+p junction of the same doping [7] For a p doping of $6x10^{15}$ /cm^3, E_c is $2x10^6$ V/cm. For this value of E_c we get an optimum dose of Q = $1.07x10^{13}$ /cm^2.

Therefore, if the RESURF phenomena is found to work for SiC, we expect a maximum breakdown voltage of 2380V which should occur at a dose of approximately $1.0x10^{13}$ /cm^2.

The Single Zone RESURF diode was simulated for various doses, using the 2-D numerical simulator, MEDICI. The RESURF phenomena can be better understood by analysis of the operation in 3 regions:

Region 1: When the dose is very high, the RESURF layer does not fully deplete on the application of a high reverse bias. In this case, therefore, electric field crowding occurs at the anode end and the device breaks down due to high fields under the anode field plate much before the parallel plane breakdown is reached. The potential distributions and the electric field profile for a high dose of $3x10^{13}$/cm^2 is shown in Fig. 2 and Fig. 3.

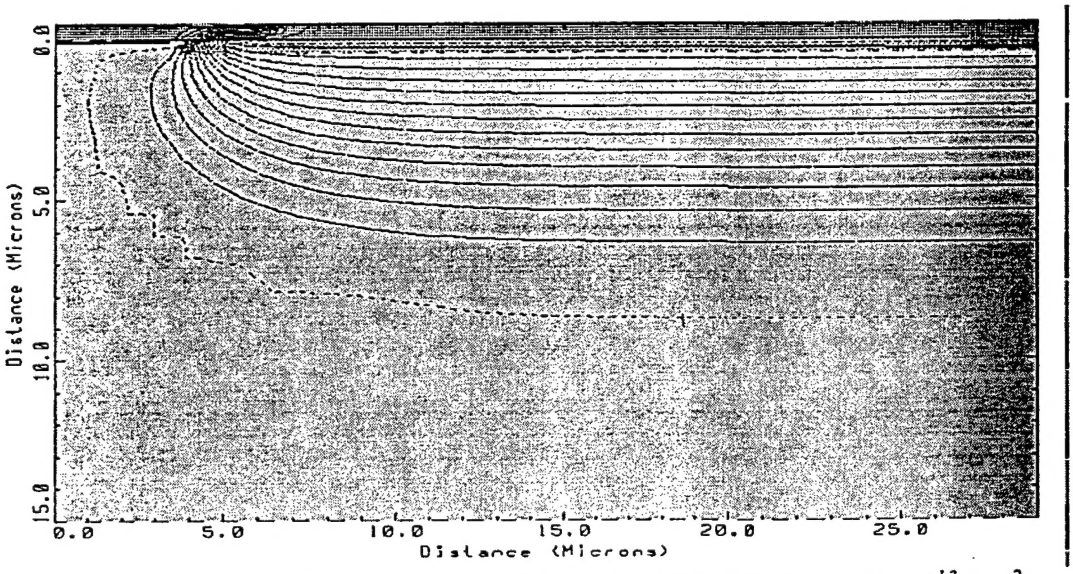


Fig 2 Potential Contours at breakdown for RESURF dose of $3x10^{13}$ /cm^2

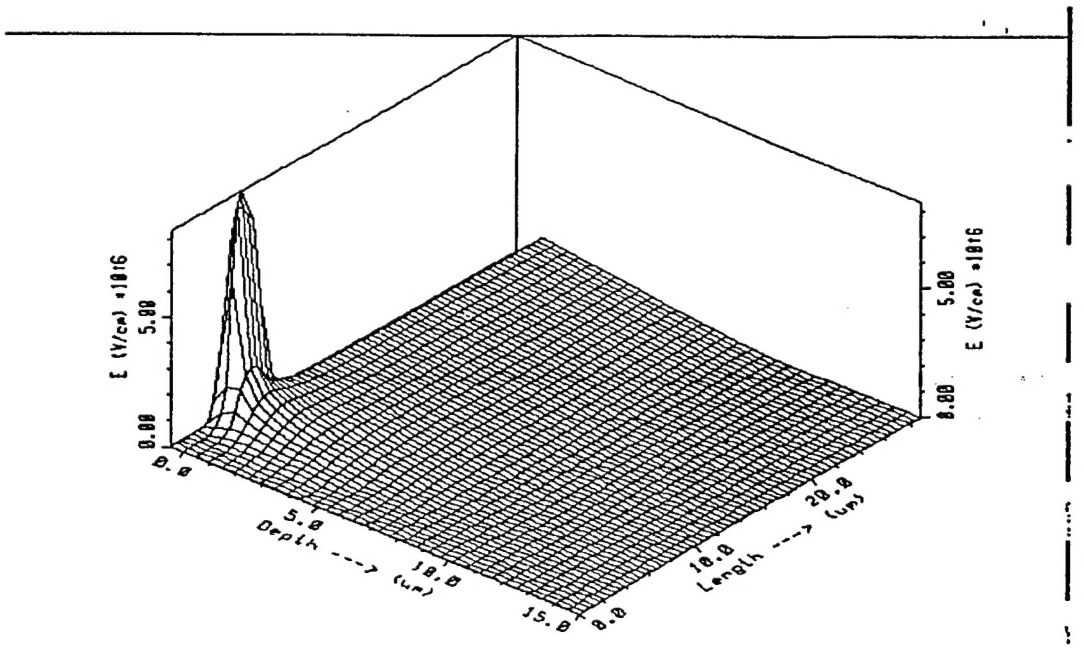


Fig 3 3-D Plot of the Electric field in the diode for a dose of $3x10^{13}$ /cm^2

The electric field along the surface in SiC is shown in Fig. 4. The plot clearly shows a very high electric field peak at the anode end. This is responsible for the early breakdown of the device. The 3-D potential distribution plot is shown in Fig 5. From the plot, we can see that most of the potential drop occurs at the anode end.

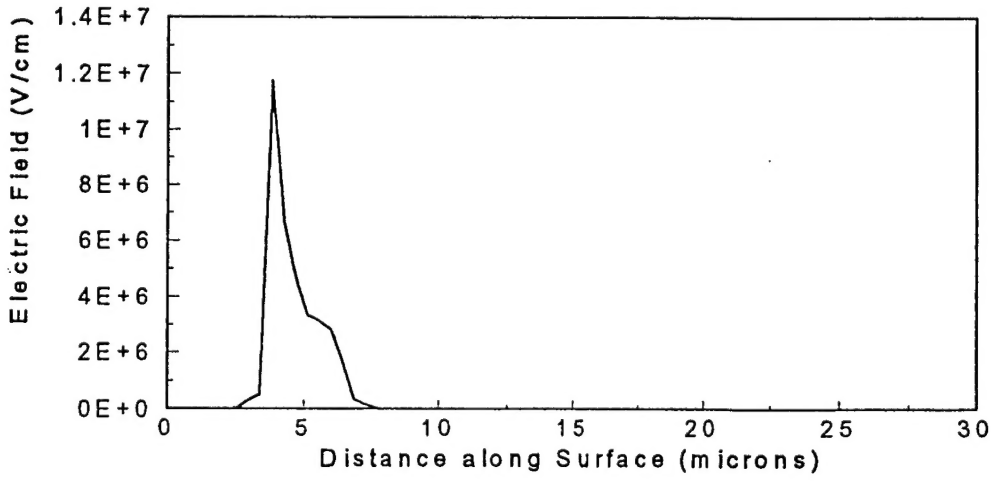


Fig 4 Electric Field Profile in the RESURF layer for a dose of $3x10^{13}$ /cm^2

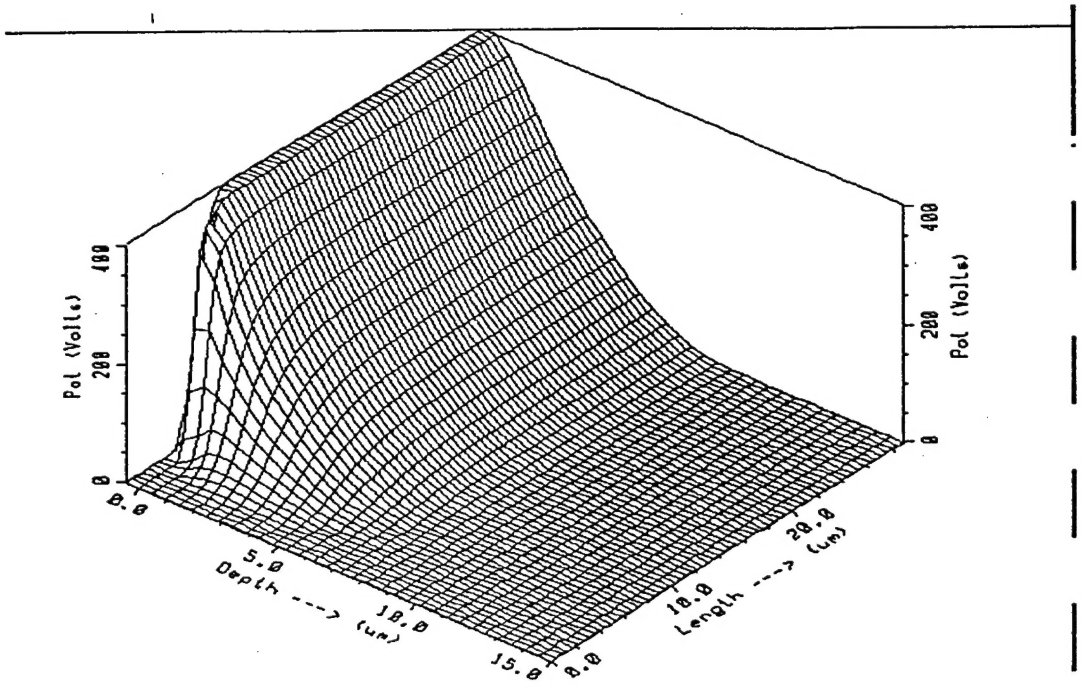


Fig 5 3-D Plot of the Potential distribution in the diode for a dose of $3x10^{13}$ /cm^2

Region 2: At very low doses, the depletion reaches the cathode end. However, due to the curvature of the N^+-N_{res} junction, electric field crowding occurs and high fields are formed at the cathode end. In this case too, the breakdown voltage is less than the optimum value. The potential distributions and the electric field profile for the low dose of $1x10^{12}$ /cm^2 are shown in Fig. 6 and Fig. 7 where the field crowding at the cathode end dominates the field crowding at the anode end.

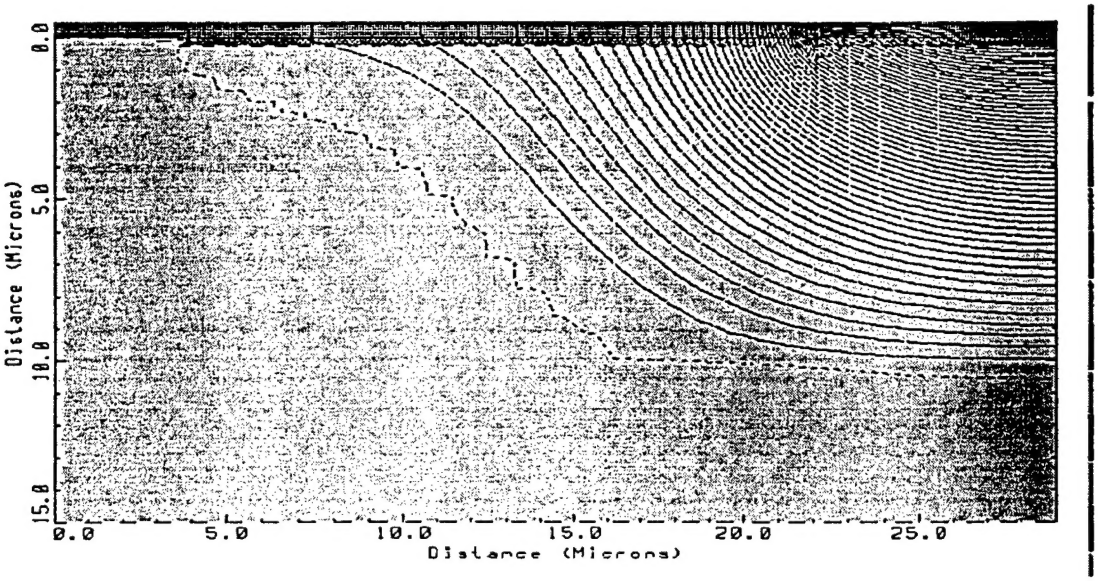


Fig 6 Potential Contours at breakdown for RESURF dose of $1x10^{12}$ /cm^2

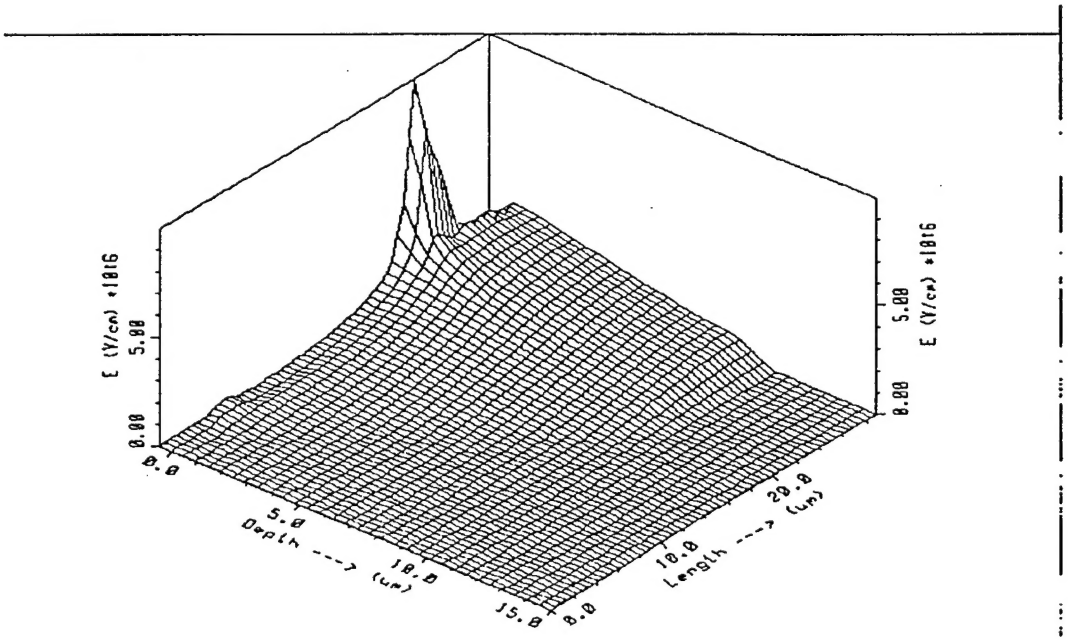


Fig 7 3-D Plot of the Electric field in the diode for a dose of $1x10^{12}$ /cm^2

The electric field at the surface is shown in Fig. 8. In this case, the peak electric field occurs at the cathode end where most of the potential drops as seen from Fig. 9

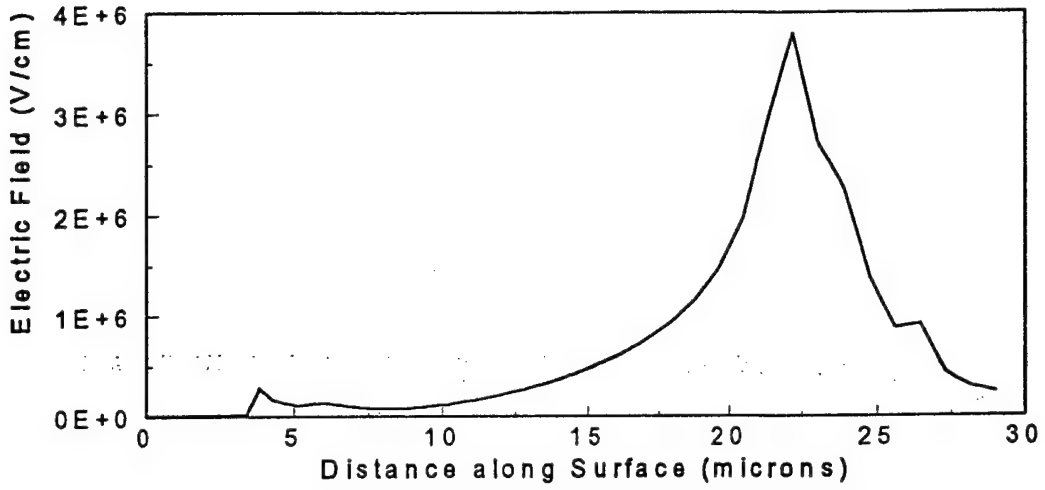


Fig 8 Electric Field Profile in the RESURF layer for a dose of 1x10^{12} /cm^2

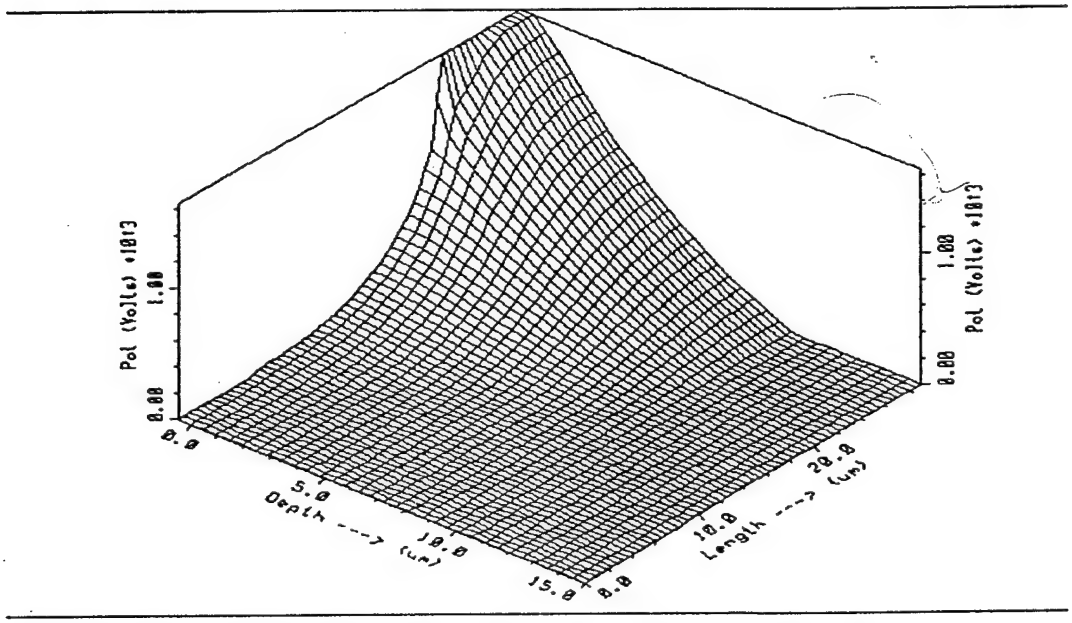


Fig 9 3-D Plot of the Potential distribution in the diode for a dose of 1x10^{12} /cm^2

Region 3: At more optimum doses, the field crowding at the anode and the cathode end are comparable. In this case, therefore, a more uniform field profile is obtained in the RESURF layer. Here again, the breakdown occurs at the drain end but if the RESURF length is sufficiently large, then the breakdown can occur at the horizontal P^-N_{res} junction and one can achieve the maximum breakdown voltage possible. The potential distributions and the electric field profile for this case (for a dose of 7x10^{12} /cm^2) are shown in Fig. 10 and Fig 11.

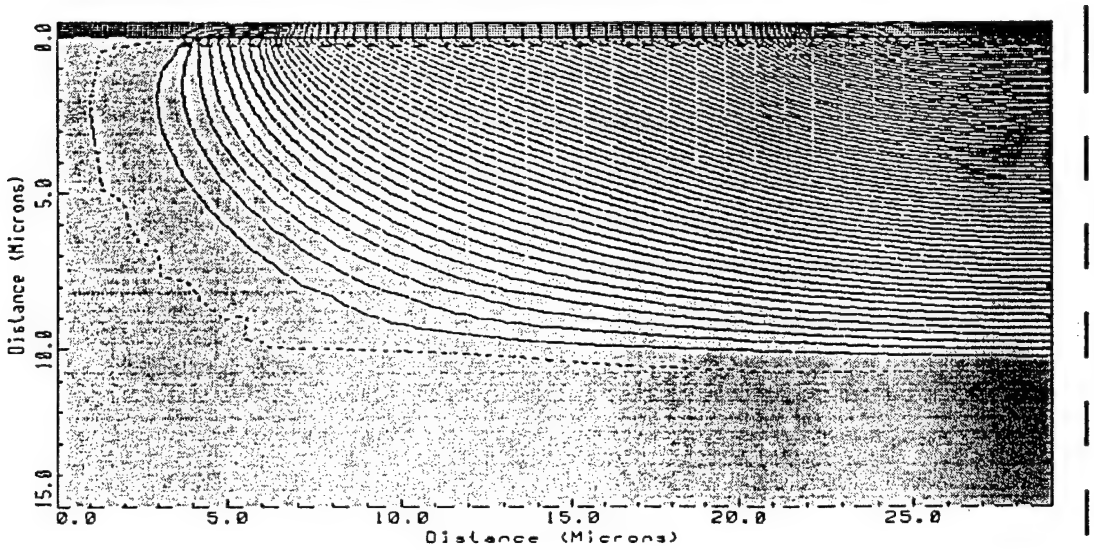


Fig 10 Potential Contours at breakdown for RESURF dose of $7x10^{12}$ /cm^2

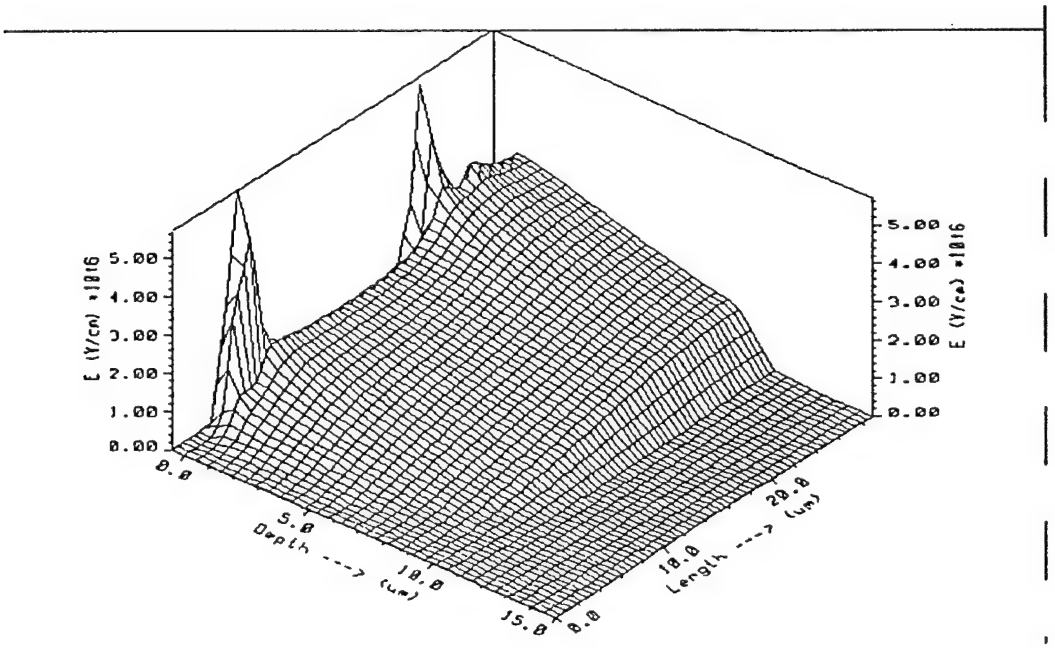


Fig 11 3-D Plot of the Electric field in the diode for a dose of $7x10^{12}$ /cm^2

The 1-D electric field profile at the surface in SiC can be seen in Fig. 12. For this optimum dose, two almost equal peaks are formed at the anode and cathode end. This kind of profile can support a higher breakdown voltage than other profiles seen in previous cases. Fig 13 shows the 3-D potential distribution for this case.

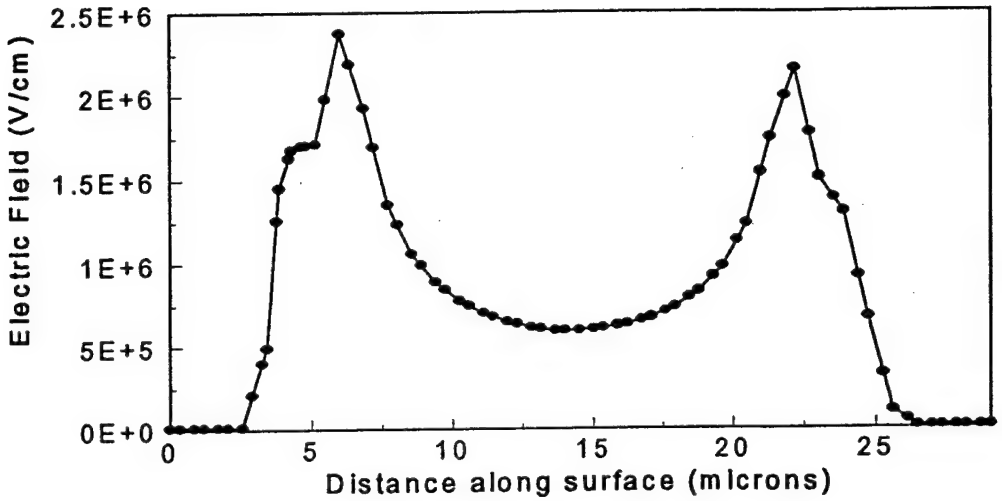


Fig 12 Electric Field Profile in the RESURF layer for a dose of $7x10^{12}$ /cm^2

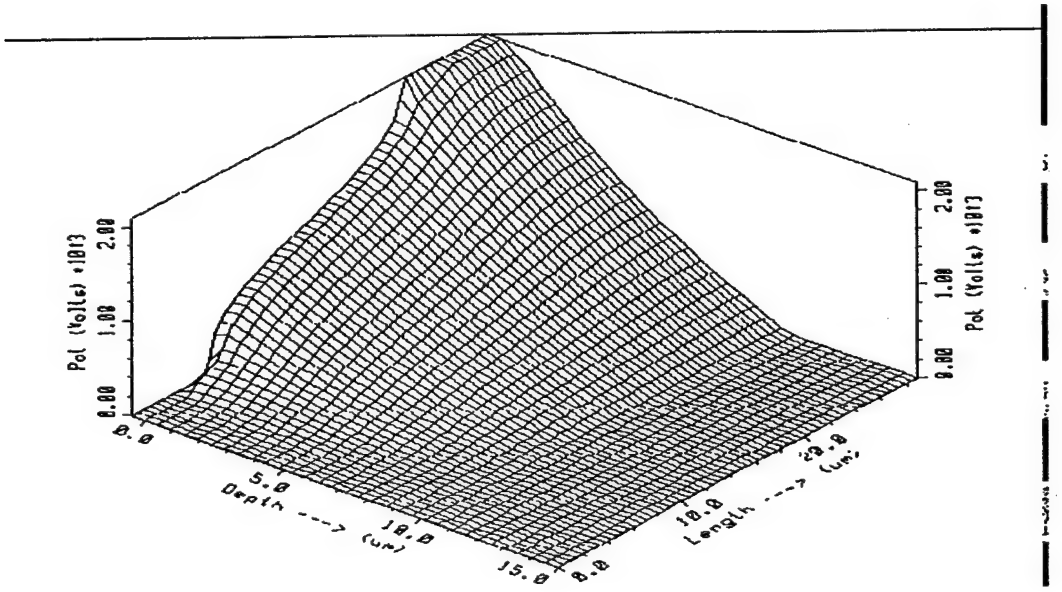


Fig 13 3-D Plot of the Potential distribution in the diode for a dose of $7x10^{12}$ /cm^2

The potential distribution along the substrate at the cathode end is shown in Fig 14. The depletion extends all the way to the epi layer and punches through to the P^+ substrate. Therefore, a higher breakdown voltage can be obtained if a thicker epi layer is chosen. However due to the current unavailability of epi layers thicker than 10 microns, we did not simulate for thicker epi layer devices.

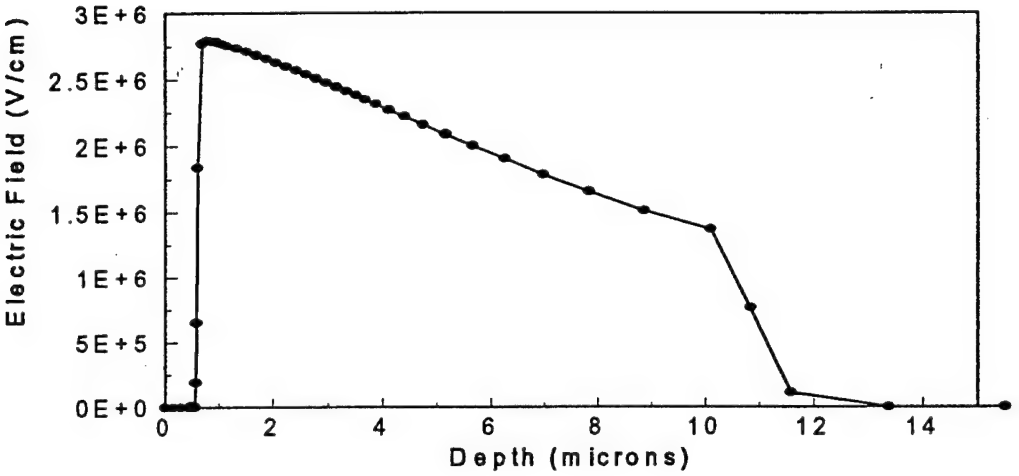


Fig 14 Electric Field Profile along the substrate (cathode end)

The breakdown voltage vs. RESURF layer dose, then follows the curve shown in Fig.15 For very high doses, the breakdown voltage is limited by the breakdown due to field crowding at the anode end and hence is quite low. At intermediate doses, better breakdown voltages are obtained due to more uniform electric field in the RESURF layer. For very low doses, the breakdown is again limited by the field crowding at the cathode end. This is again lower than the ideal parallel plane breakdown though not as low as for high doses.

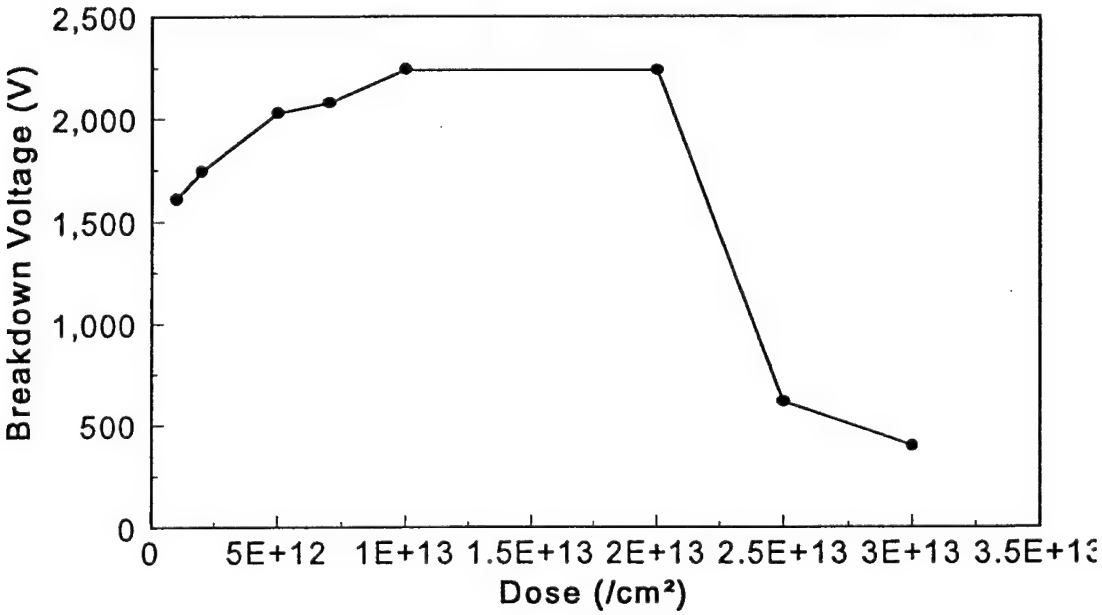


Fig 15 Dose vs. Breakdown Voltage for the single zone RESURF diode

From our simulations, the maximum breakdown voltage that we obtained was 2240V at a dose of $1x10^{13}$ /cm^2 which is around 94% of the ideal parallel plane breakdown voltage. For comparison, the ideal parallel plane breakdown voltage for the same epi layer doping of $6x10^{15}$/cm^3 is around 300V for Si.

Simulations were also performed for different lengths of the RESURF layer. As the length is increased, the breakdown voltage increases linearly till it reaches the ideal parallel plane breakdown voltage, after which it saturates. Further increase in the length of the RESURF layer does not increase the breakdown voltage appreciably. This can be seen from Fig.16, from which the optimum length is found to be 15μ. All the simulations for this were done for the dose of $1x10^{13}$ /cm^2.

For the dose of $1x10^{13}$ /cm^2, where maximum breakdown occurs, the breakdown occurs at the cathode end. The breakdown voltage can be expected to be affected by the position of the cathode field plate position. Therefore, we ran simulations for various field plate lengths. The simulation results are shown in Fig. 17. From the simulation results, we find that in this case, the field plate length does not play a critical role in determining the breakdown voltage of the device.

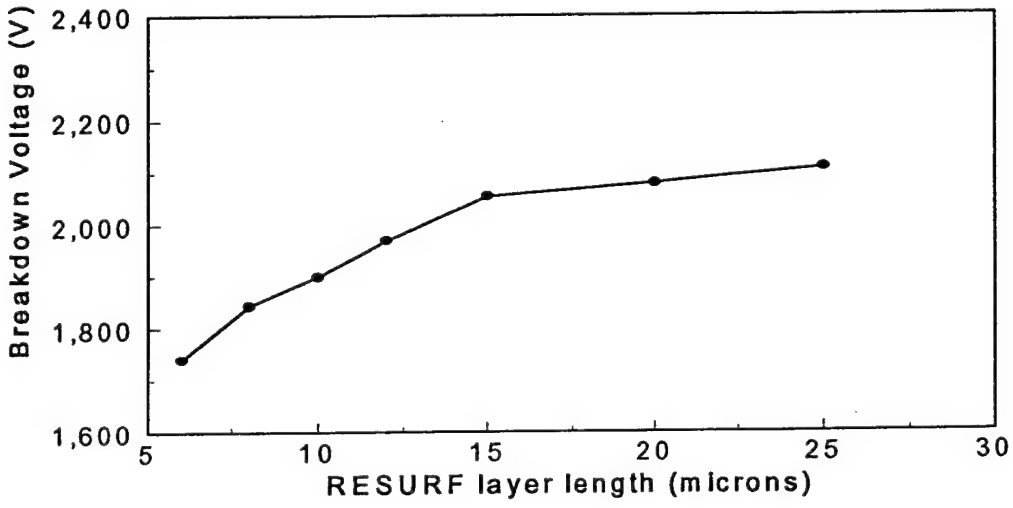


Fig 16 Breakdown Voltage obtained for different RESURF lengths (L_R)

Though this field is less than the oxide rupture field, it is still high enough to make these devices unreliable. One of the solutions to this problem is to use an insulator with a dielectric constant higher than that of oxide. For instance, Silicon Nitride has a dielectric constant
of 7.5 as compared to oxide whose dielectric constant is 3.9. This means that a field of $7x10^6$ V/cm in oxide would correspond to a field of around $3.7x10^6$ V/cm in nitride. The nitride rupture field being the same as that of oxide, this would mean that more reliable devices can be fabricated using nitride rather than oxide. Consequently, simulations were done using nitride as the dielectric and these results are discussed next.

Simulations using Nitride as the dielectric

Simulations were repeated for the structure shown in Fig.1 with nitride in place of oxide. All other parameters were kept the same. The RESURF diode exhibits similar regions of operations as in the oxide case. In region 1, when the dose is very high, breakdown occurs at the anode end due to electric field crowding under the anode. The potential distribution for this case is shown in Fig 19.

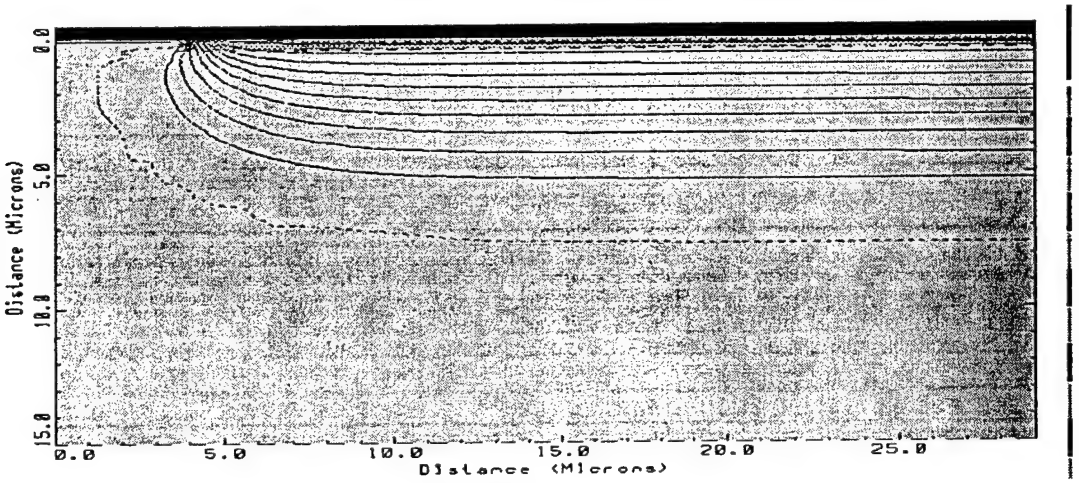


Fig.19 Potential Contours at breakdown for RESURF dose of $3x10^{13}$ /cm^2

The electric field profile in the device and along the surface are shown in Fig. 20 and Fig. 21. A very high peak can be observed in the anode region which is responsible for an early breakdown of the device.

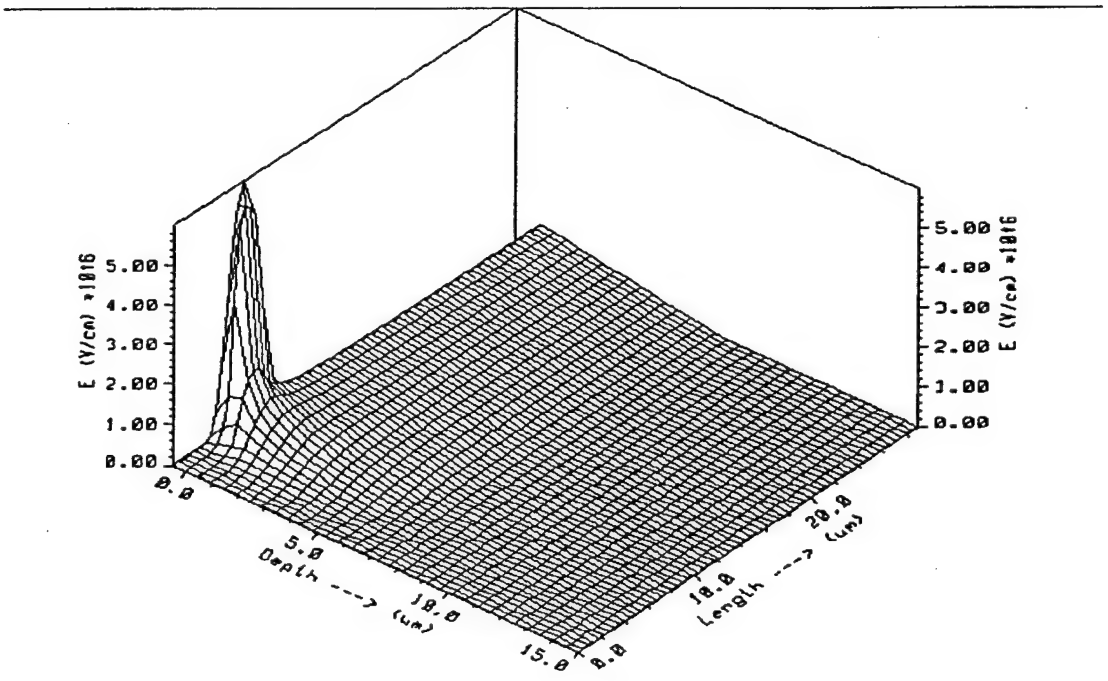


Fig 20 3-D Plot of the Electric field in the diode for a dose of $3x10^{13}$ /cm^2

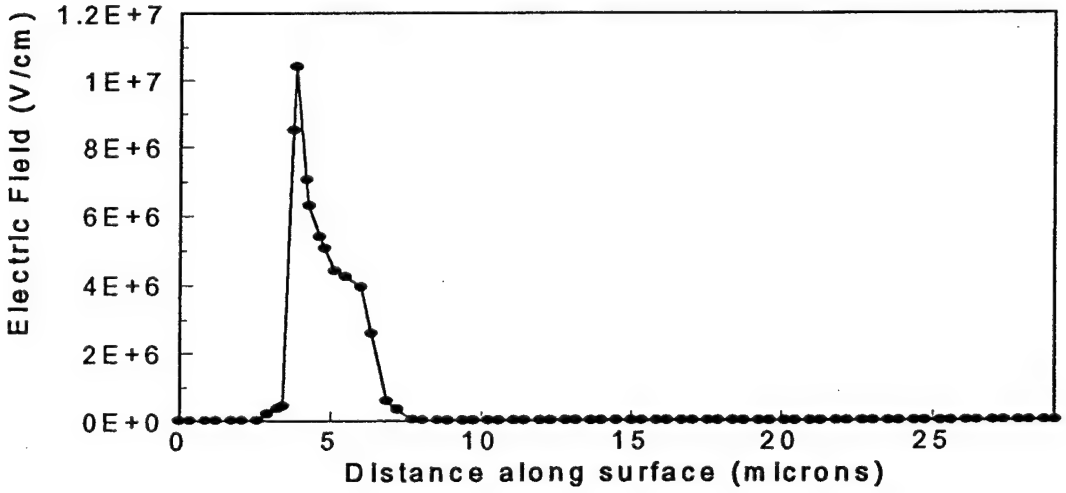


Fig.21 Electric Field Profile in the RESURF layer for a dose of $3x10^{13}$ /cm^2

Fig 22 shows the potential distribution in the device and once again we see a large potential drop at the anode end.

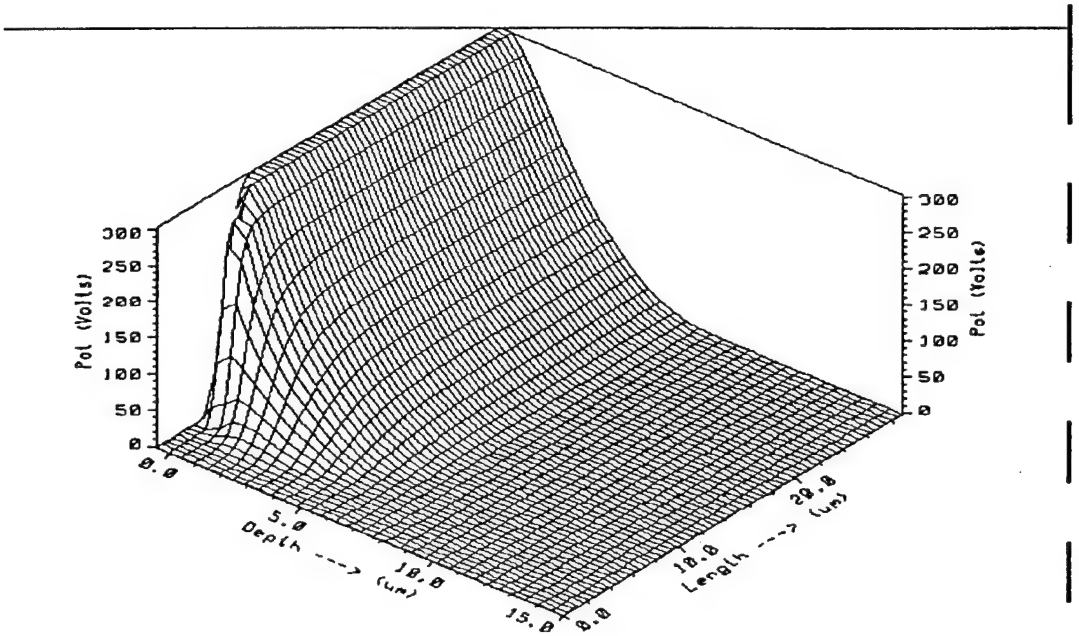


Fig 22 3-D Plot of the Potential Distribution in the diode for a dose of $1x10^{12}/cm^2$

Region 2 shows the other extreme with electric field crowding at the cathode end for a very low dose. The breakdown voltage is again less than optimal as expected. The potential distributions and the electric field distribution in the device are shown in Fig.23 and Fig. 24.

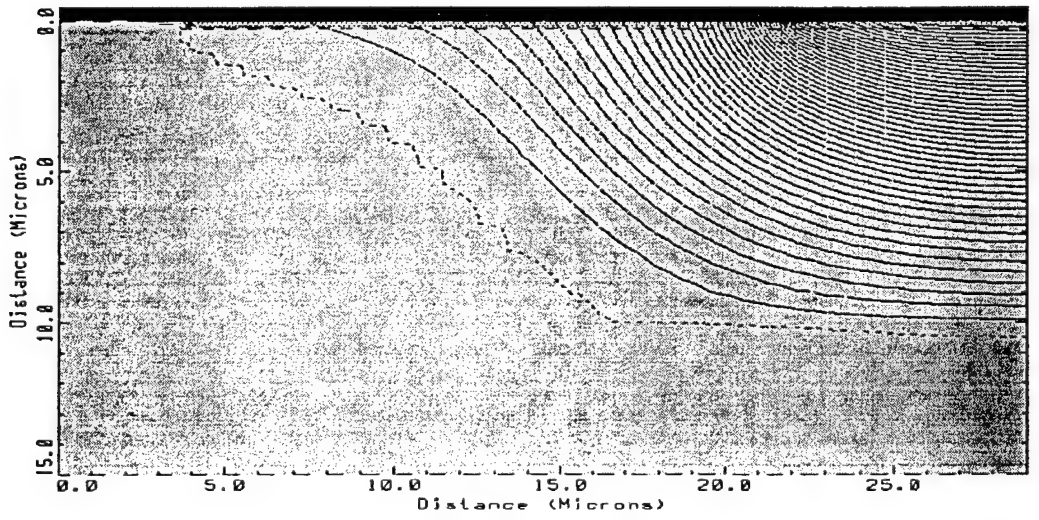


Fig.23 Potential Contours at breakdown for RESURF dose of $1x10^{12}$ /cm²

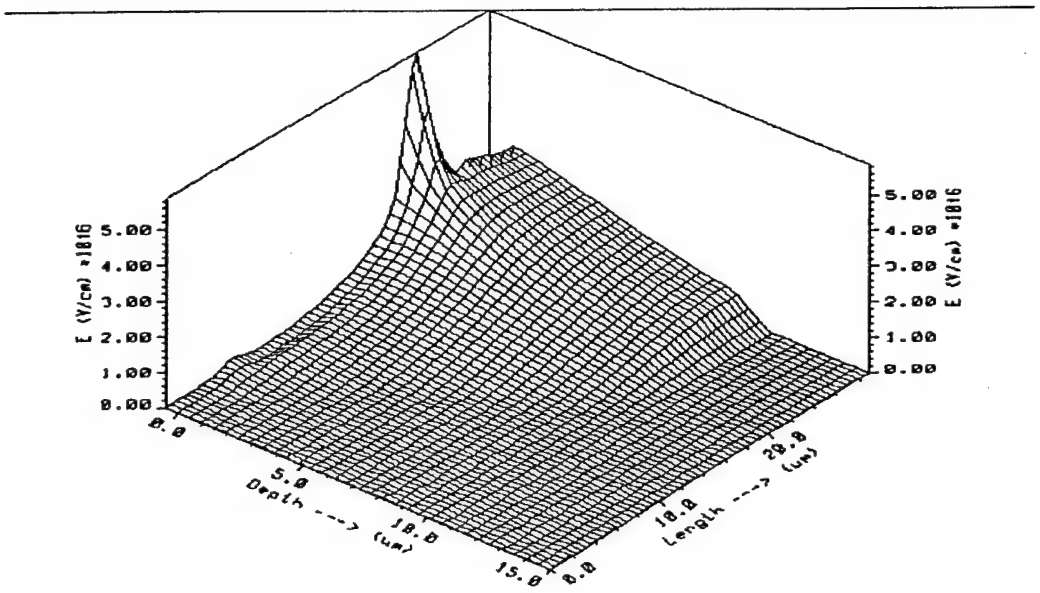


Fig 24 3-D Plot of the Electric field in the diode for a dose of 1x10^{12} /cm^2

The 1-D electric field profile for this case is shown in Fig. 25 and the potential distribution in the device is shown in Fig. 26. Both the plots indicate high electric fields at the cathode end which leads to an early breakdown of the device.

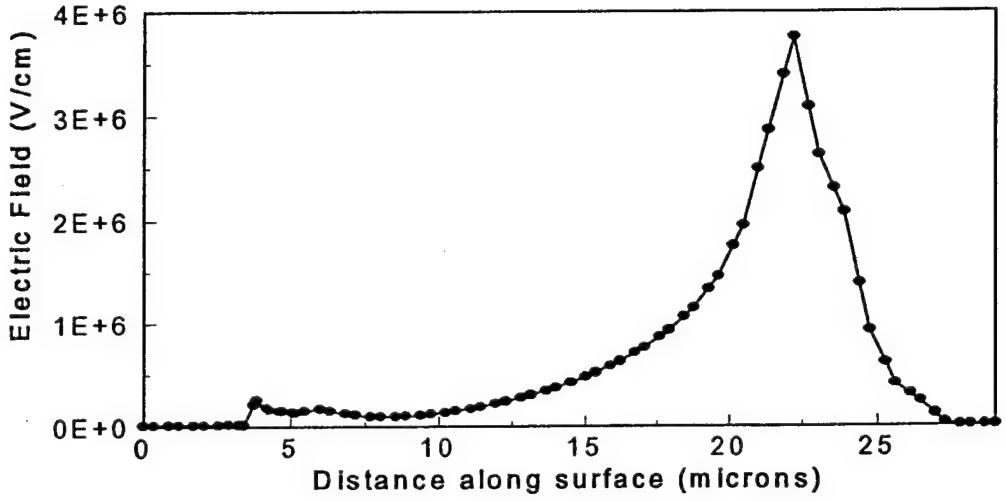


Fig.25 Electric Field Profile in the RESURF layer for a dose of 1x10^{12} /cm^2

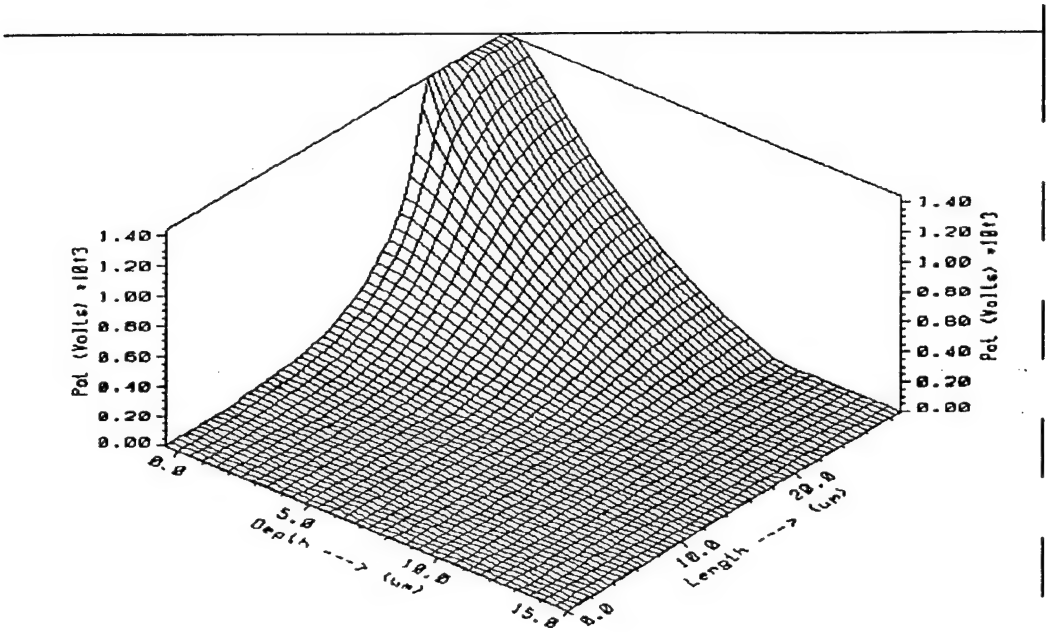


Fig 26 3-D Plot of the Potential distribution in the diode for a dose of $1x10^{12}$ /cm^2

Region 3 corresponds to the optimal case, where the electric field is more uniformly distributed in the RESURF layer. Two peaks of the electric field occur at both the anode and the cathode end. Due to the more uniform electric field profile, the breakdown voltage is higher in this case as explained before. The potential distributions and the electric field profile for this region of operation are shown in the following figures.

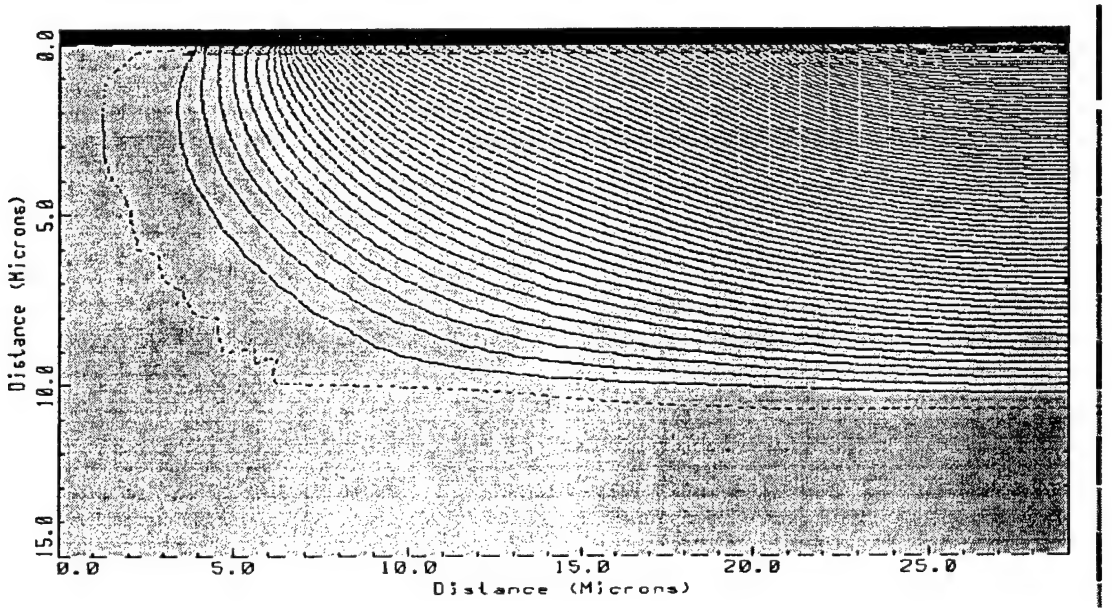


Fig.27 Potential Contours at breakdown for RESURF dose of $7x10^{12}$ /cm^2

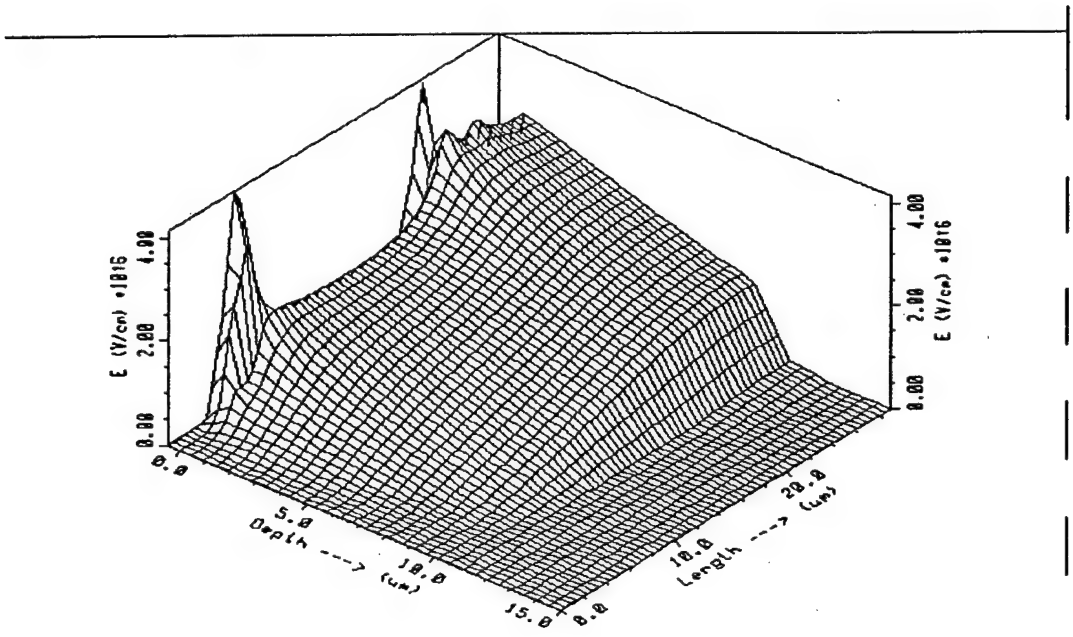


Fig 28 3-D Plot of the Electric field in the diode for a dose of $7x10^{12}$ /cm^2

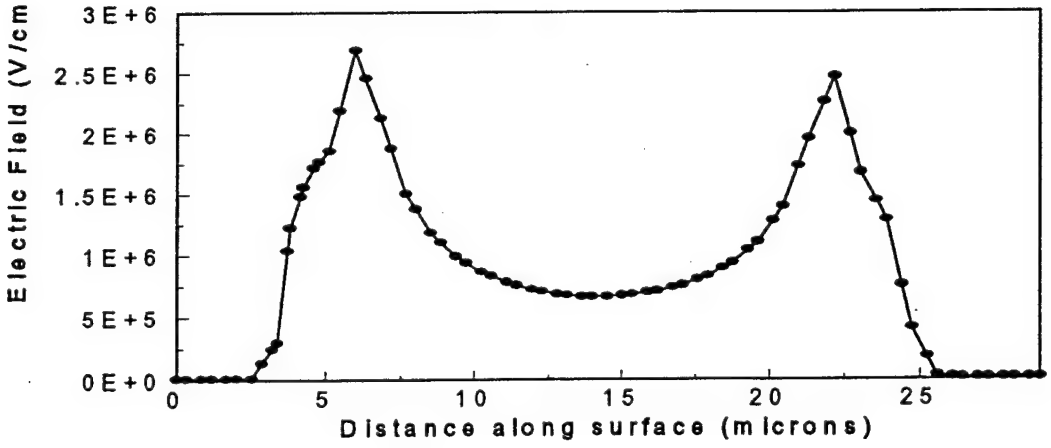


Fig. 29 Electric Field Profile in the RESURF layer for a dose of $7x10^{12}$ /cm^2

Both Fig 28 and Fig 29 clearly show 2 electric field peaks at both the anode and the cathode end. As in the oxide case, this kind of profile gives a better breakdown voltage. The potential distribution in the device is shown in Fig. 30 for this case.

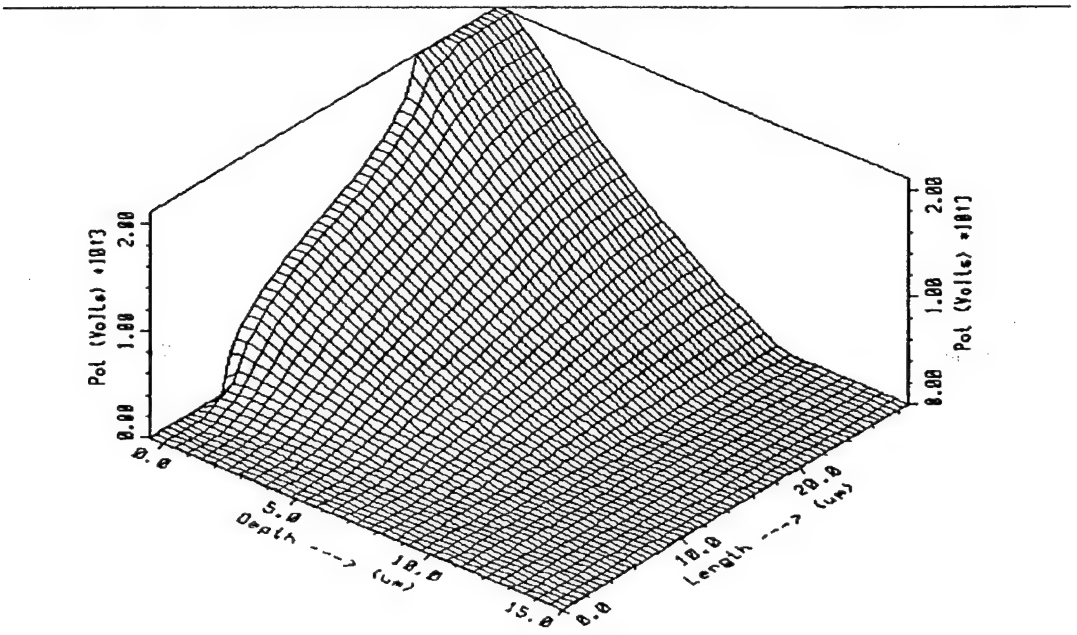


Fig 30 3-D Plot of the Potential distribution in the diode for a dose of $7x10^{12}$ /cm²

For the nitride simulations, the optimum dose was found to be $7x10^{12}$ /cm² which gave the maximum breakdown voltage of 2100V. This is around 150V lesser than the maximum breakdown voltage that was obtained for the oxide simulations. The breakdown voltage for different RESURF doses is shown in Fig. 31.

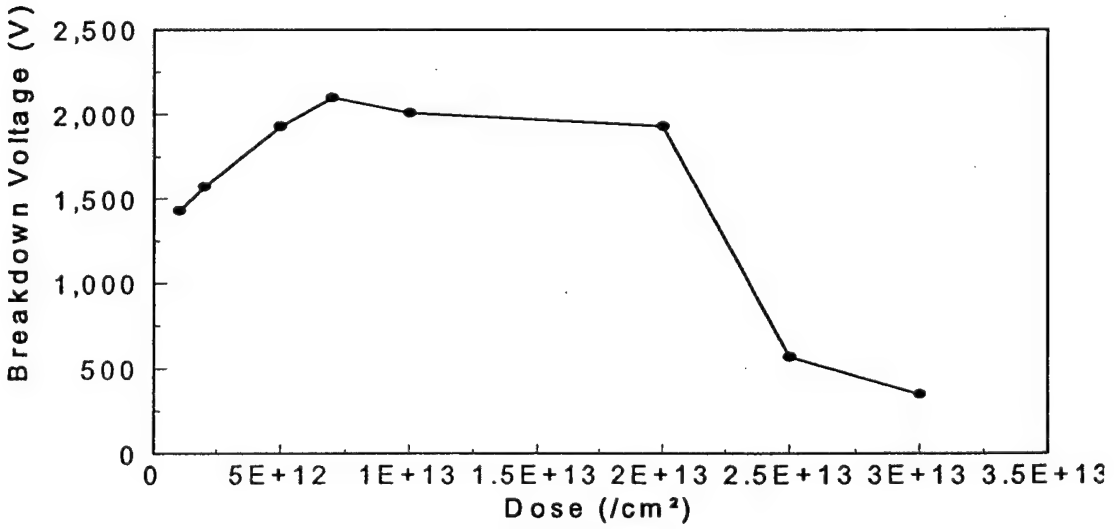


Fig. 31 Dose vs. Breakdown Voltage for the RESURF diode with nitride as dielectric

For the optimum case where we get the maximum breakdown voltage, the corresponding electric field in the nitride is shown in Fig 32.In this case, the maximum electric field in the nitride is less than half the field in the oxide case. The electric field in nitride doesn't exceed $3.5x10^6$ V/cm which is much less than the nitride rupture field of $1x10^7$ V/cm Therefore, devices made with nitride as the dielectric should turn out to be more reliable than devices made in oxide for very high voltage devices.

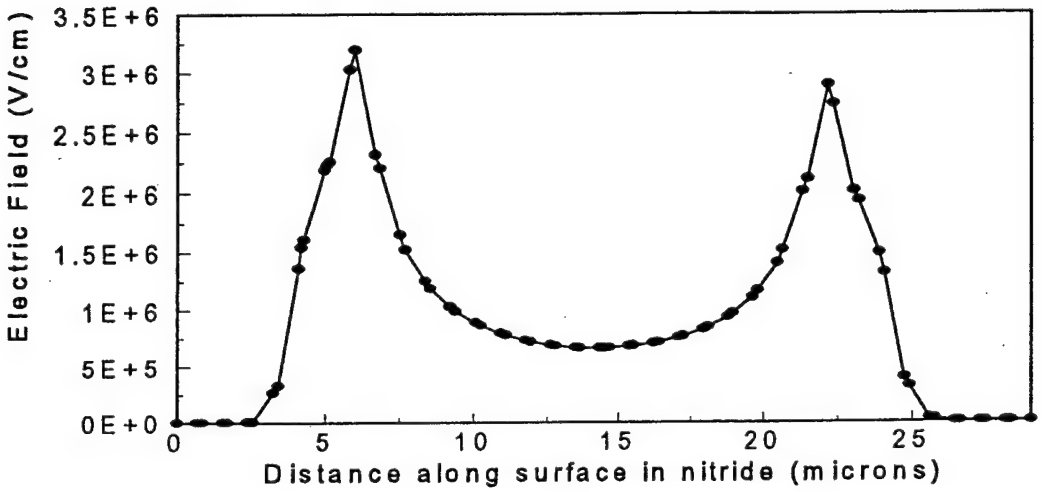


Fig.32 Electric Field in nitride for a RESURF dose of $7x10^{12}$ /cm^2

Conclusions

Extensive numerical simulations were performed to study the breakdown voltage of the single zone RESURF diode with both oxide and nitride as the dielectric. For the oxide, we obtained the maximum breakdown voltage of 2240V which was at a dose of $2x10^{13}$ /cm^2 . The maximum electric field at this dose in the oxide was around $7x10^6$ V/cm. This is a reasonably high electric field, even though it is less than the oxide rupture field of $1x10^7$ V/cm. This could possibly make devices unreliable. To solve the problem of high fields in oxide, we decided to replace the oxide with nitride which has a lower dielectric constant. Simulations with nitride as the dielectric indicate the maximum electric field in nitride to be less than $3.5x10^6$ V/cm, which is much less than the nitride rupture field of $1x10^7$ V/cm . The maximum breakdown voltage that we obtained for the nitride case was 2100V at a dose of $7x10^{12}$ /cm^2 . For both oxide and nitride cases, we obtained a good range ($7x10^{12}$ /cm^2 - $2x10^{13}$/cm^2) of dose where the breakdown voltage is quite high (2000V and above). A high breakdown voltage at a high dose of $2x10^{13}$/cm^2 implies that devices like RESURF MOSFETs can be fabricated, which will exhibit a high breakdown voltage and a low specific on-resistance.

References

1) B.J. Baliga, *Technical Digest Int. Conf. On SiC and Related Materials (ICSCRM '95)* pp 3-4
2) S. Merchant et al, *Proc. 3rd Int. Symp. On Power Semiconductor Devices and ICs (ISPSD)*, pp 31 (1991)
3) Zahir Parpia and Andre T. Salama, *IEEE Transactions on Electron Devices*, Vol 37, pp 789-796, (1990)
4) R. Sunkavalli et al, *Tech. Report, PSRC Document:TR-96-016*, (1996)
5) D.Alok and B.J. Baliga, *Electronics Letters*, Vol. 33, No. 20, pp 1929-1931, (1996)
6) J.A. Appels and H.M.J. Vaes, *IEDM Tech. Digest*, pp 238 (1979)
7) John Palmour and Lori Lipkin, *Trans. on 2nd Int. High Temp. Elec. Conf.*, Vol. 1, pp XI-3 - XI-8, (1994)

Silicon Carbide High Voltage Lateral RESURF MOSFETS and RESURF Diodes

S. Sonkusale, A. Venkateswaran, P. Mehrotra and B.J. Baliga.
Power Semiconductor Research Center
North Carolina State University
Raleigh NC 27695,USA
Phone: (919)-515-6166 Fax: (919) 515-6170

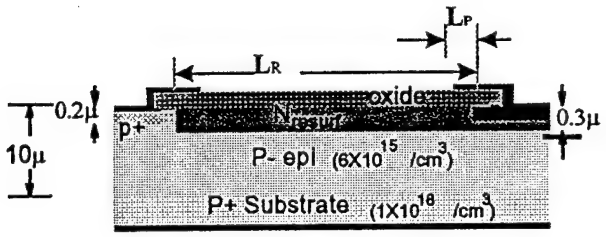
Abstract

Silicon Carbide is an attractive material for the development of high voltage , high temperature and high frequency devices . SiC has the critical field ten times higher than that of the silicon . This implies that lateral RESURF devices made in SiC can support the same breakdown voltage in a much smaller drift length as compared to the silicon devices. In our project we are using the concept of Lateral RESURF device to obtain diodes and MOSFETs having high breakdown voltage and small specific on-resistance. In this report I have given the brief explanation of fabrication process and the issues involved.

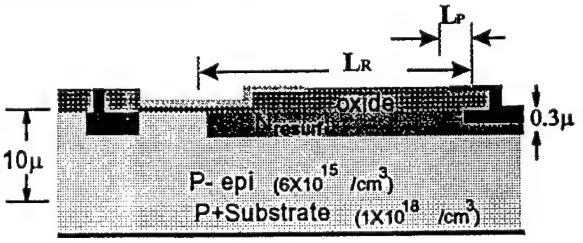
I. INTRODUCTION

The goal of this project is to apply RESURF principle to get high voltage devices in SiC. In this project we are focusing on 4H- SiC to determine the optimum RESURF dose and RESURF layer length to get high breakdown voltage and minimize the specific on-resistance . From the results of two dimensional numerical simulations on the RESURF devices ,it was found that in RESURF diodes high breakdown voltage (>2000 V) is possible for the RESURF dose of up to 2 x 10^{13} cm^{-2} ,which is 10-20 times higher than for silicon devices. Also in LATERAL RESURF MOSFETs high breakdown voltage (>1800)was possible for RESURF dose of up to 1 x 10^{13} cm^{-2} ,which is 5-10 times higher than for silicon MOSFETs. The specific on resistance of these devices was found to be less than 100 mohm- cm^2. Based upon this mask set of 11 masks with various RESURF layer length and field plate lengths was designed to provide experimental verification. A mask layout (using 2 micron design rules) was designed with an array of diodes and MOSFETs (both inversion and accumulation type) using layout editor LTL. Various diagnostic test elements like Hall elements for mobilities , Van der Pauw structures for sheet resistance ,TLM structures for contact resistance and capacitors are also included .The first run has only single zone RESURF devices.

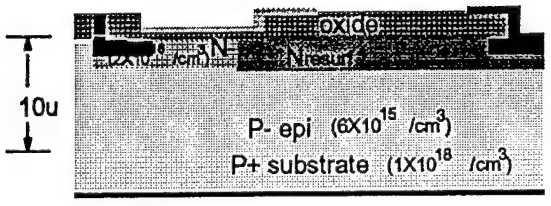
II. LATERAL RESURF SRTUCTURES



Lateral RESURF Diode

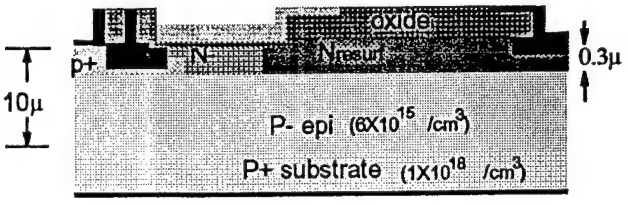


Lateral RESURF Inversion MOSFET



$W_{n,max}$ = 0.189μ

Lateral RESURF Accumulation MOSFET



$W_{n,max}$ = 0.396μ

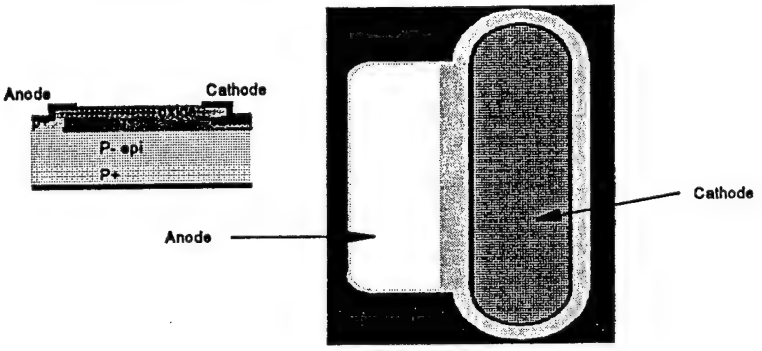
➡ With p+ layer, depletion pushed to n- side

Lateral RESURF Accumulation MOSFET with p+ burried layer

In first run we are fabricating single zone RESURF diodes and LATERAL RESURF MOSFETs, Inversion as well as Accumulation MOSFETs, on 4H-SiC substrate. From MEDICI simulations of these devices it was found that Breakdown voltage is low for very high and very low RESURF layer doping. However ,for the given range of optimum RESURF layer doping we get very high Breakdown voltage. Breakdown voltage also increases with the increase in the RESURF layer length. It was also concluded that Breakdown voltage does not change much with the change in field plate length. Hence, simulation were carried out to find the optimum RESURF layer dose and RESURF layer length .Based upon this, devices are fabricated at PSRC, with varying RESURF layer doses , RESURF layer length and Field plate length.

III. Mask Layout and Device Design Matrix

Layout of the Single Zone RESURF Diode

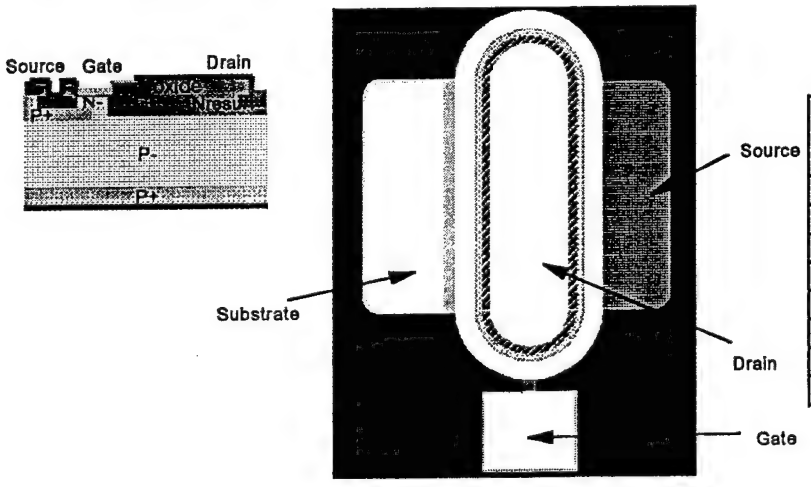


Racetrack Design

Design Matrix

No.	$L_R(u)$	$L_P(u)$
1	5	3
2	10	3
3	15	3
4	20	3
5	25	1
6	25	2
7	25	3
8	25	4
9	30	3

Layout of the Single Zone RESURF MOSFET



Racetrack Design

Design Matrix

No.	$L_R(u)$	$L_P(u)$
1	10	3
2	15	3
3	20	3
4	25	2
5	25	3
6	25	4
7	30	3
8	35	3

The mask layout was designed in 'LTL-100' layout design software with 2 μm design rules. Racetrack design is used to reduce electric field crowding at the edge and hence improving the blocking voltage capability. The RESURF layer length is varied from 5μ m to 30μm for diodes and

10μ to 35μ for MOSFETs. Also Field plate length is varied from 1μ m to 3μ m. Diodes and MOSFETs for two different RESURF layer dose are fabricated on the same SiC substrate.

Test elements like Hall elements for mobility measurement, Van der Pauw structures for sheet resistance ,TLM structures for contact resistance measurement and capacitors were also fabricated on device. Apart from these some aggressive designs using stricter design rules have been added.

IV. PROCESS FLOW AND DEVICE FABRICATION

A 11 mask process was defined to fabricate the RESURF Diodes and LATERAL RESURF MOSFETs. The process parameters were determined by the process simulation using SUPREM IV as well as by test runs. The detailed description of process is given in Table 1. The names and types of masks is given in Table 2.. It also summarizes the type of photoresist (positive and negative) used with each mask level, and levels matched while drawing alignment patterns on the layout. Fig 1 shows the final cross-section of the devices.

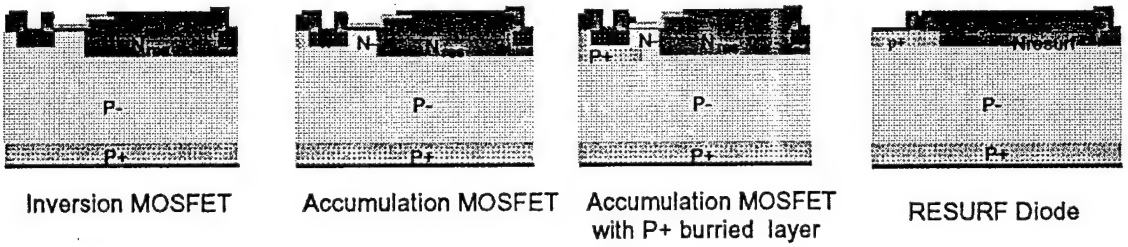


Figure 1. **Cross-section of final devices.**

The starting wafers for 4H-SiC were single crystal P type substrates (1×10^{18} /cm^3) with 10μm thick P epi layer (6×10^{15} /cm^3). All the wafers were initially cleaned using a five minute dip in JT baker clean solution. The first mask level was designed to etch alignment marks on the SiC wafers. The alignment marks etched into SiC by reactive ion etching (RIE) using photoresist as the mask. The following procedure was used. After JTB clean ,all wafers were dried on a hot plate at 115 °C for 5 min. Next, hexamethyldisilizane (HMDS) and then , the photoresist were spun on the wafers ,each at the speed of 4500 rpm and for 40 sec. The wafers were baked (pre-expose bake) at 90 °C for 1 min. Then, the wafers were exposed using the first mask level on the Karl Suss MJB3 contact printer at the intensity of 15 mW/cm^2 for 30 seconds in a constant power mode. After a post-exposure bake at 115 °C for 1 minute, the patterns were developed using a minute dip in developer solution. A post develop bake at 90 °C was done for 1 minute to reduce the moisture content on the wafers. The RIE was performed using Oxford Plasmalab system . SiC was etched using a mixture of sulfur hexafluoride (SF_6) at 9 sccm and oxygen (O_2) at 1 sccm for 8 minutes at a power of 120 W, a pressure of 50 mTorr and temperature of 15 C. This recipe gave high etch selectivity of SiC to Photoresist and ensured proper masking while etching. This process resulted in SiC alignment marks that were approximately 0.25-0.3 μm deep. After RIE the photoresist was stripped from the wafers using a ten minutes dip in Nanostrip solution .Any remnants of PR were removed using a room

temperature oxygen plasma in an Asher by March Instrument at 300 W and 600mTorr at an oxygen flow of 80 sccm. Then the wafers were cleaned using JT Baker clean solution.

The second mask level was used for creating the buried P+ layer on the wafers. The buried junction was formed by boron implantation using a 1.6 μm thick oxide as mask. This thick oxide was deposited using plasma enhanced chemical vapor deposition (PECVD) in an Oxford Plasmalab 90 system using nitrous oxide (N_2O) at 710 sccm and 2% mixture of silane in helium (He) at 170 sccm, at a power 20 W, a pressure of 1 Torr, and a substrate temperature of 300 C. The SiC wafers were loaded at room temperature into the PECVD chamber to reduce thermal stress on the wafers. After oxide deposition , the second level mask was used to pattern PR on the wafers using the standard procedure as described in the previous paragraph. Next, to open windows for high energy boron implants ,approximately 1.3 - 1.4 μm of 1.6 μm thick oxide was etched by RIE using a PR as a masking material and the remaining oxide was removed by a dip in buffered oxide etch (BOE) solution. RIE of the oxide was done using a mixture of trifluoromethane (CHF_3) at 25 sccm and Argon (Ar) at 25 sccm for 45 minutes at a power of 100 W, a pressure of 60 mTorr and a temperature of 20 °C. This combination of RIE and BOE ensured less undercut of oxide and better feature size on the wafer without harming the substrate.After stripping the PR ,the wafers were sent to Implant Sciences for boron implants at 1000 °C at an energy of 380 keV, a dose of 1×10^{14} /cm^2 and a 0° tilt angle. The dose and the energy values for obtaining the buried P+ layer were determined by ion-implantation simulations. Hot implantation is done to improve activation of the dopants. The cross-section of the devices after P+ buried implants are shown in Fig.2

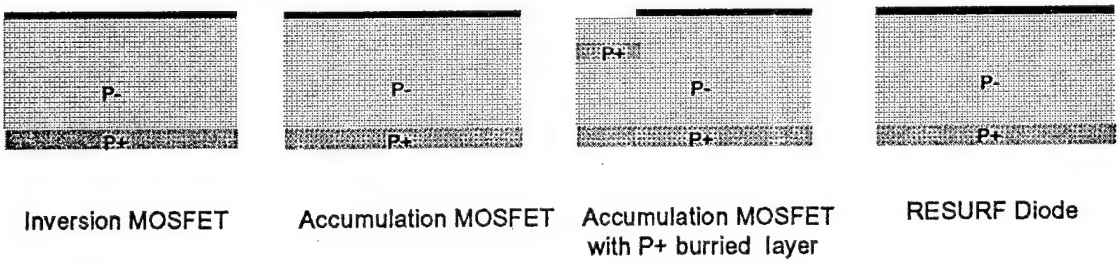


Figure 2. **Cross-section of devices after P+ burried implants.**

The third mask level was used for creating the P+ sinker layer on the wafers for making contact to the P+ buried layer. The sinker layer was formed by aluminum implantation using a 1 μm thick deposited silicon dioxide as a mask . This thick oxide was also deposited by PECVD in an Oxford Plasmalab 90 system using the same recipe as described in previous paragraph. After oxide deposition, the third level mask was used to pattern PR on the wafers using the standard procedure as described in previous paragraph. Next, to open windows for the high energy boron implants, most of thick oxide was etched by RIE using the above-mentioned recipe with PR as the masking material and remaining oxide was removed by a dip in a buffered oxide etch (BOE) solution. After stripping the PR, the wafers were sent to Implant Sciences for multiple low energy aluminum ion implants. Implants were done at 1000 °C at the energy and dose combinations of 25 keV ,4×10^{15} cm^{-2}, 75 keV, 1×10^{15} cm^{-2} , and 250 keV, 8×10^{14} cm^{-2}; and a 0° tilt angle. Multiple low energy aluminum ion implants gives smoother profile of dopants. Aluminum ion implantation is done instead of Boron Ion

implants because aluminum has lower ionization energy and so it gives higher carrier concentration and better conductivity. The cross-section of the devices after p+ sinker implants are shown in Fig. 3

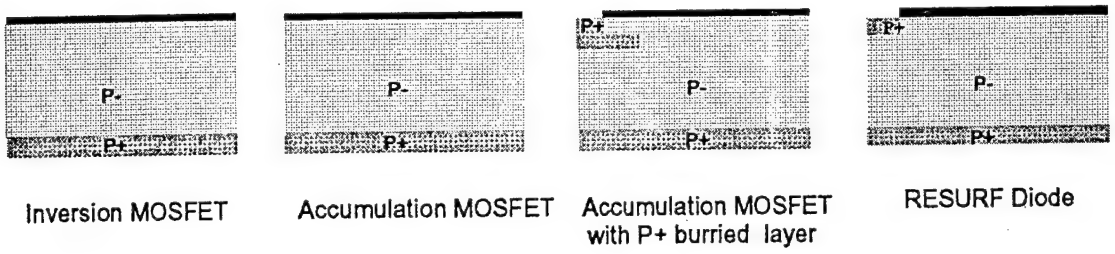


Figure 3. **Cross-section of devices after P+ sinker implants**

The fourth mask level was used for creating the N- layer on the wafers. The N- layer was formed by nitrogen implantation using photoresist as the mask. After aluminum implants, approximately 1.1 μm of the oxide was etched by RIE to the depth of 0.8 μm and rest in BOE solution, to open windows for nitrogen ion implants. The oxide was etched using photoresist as a mask which was patterned with mask 4 using standard procedure as before. The wafers were sent for Nitrogen ion implant at 1000 °C energy and dose combination of 150 keV and 5 x 10^{11} cm^{-2} and a 0° tilt angle. The cross-section of the devices after N- implants are shown in Fig. 4

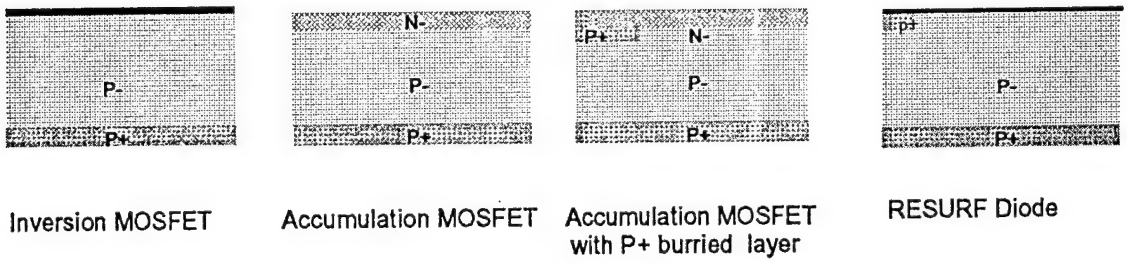


Figure 4. **Cross-section of devices after N- layer implants**

The fifth mask level was used for creating the N_{RESURF} layer on the wafers. Oxide of thickness 1 μm was deposited in LPCVD using the same recipe as used in earlier steps. The photoresist on top of this oxide was patterned using mask 5. The oxide was etched using photoresist as a mask by RIE to the depth of 0.8 μm and rest in BOE solution. Devices with two different RESURF layer dose were fabricated on the same SiC wafer. This was achieved by using the wafer split ion-implantation method. In this method , first only one half of the wafer is implanted with nitrogen ion at 1000 °C , energy 250 keV ,0° tilt angle and say dose X. Later the entire wafer is doped again with nitrogen ion at 1000 °C ,energy 250 keV and same dose X. This gives us devices with two different RESURF layer dose on the same SiC wafer. The RESURF layer doses obtained on devices were 1 x 10^{12} cm^{-2}, 2 x 10^{12} cm^{-2},3 x 10^{12} cm^{-2} ,6 x 10^{12} cm^{-2},8 x 10^{12} cm^{-2},1.6 x 10^{13} cm^{-2},2 x 10^{13} cm^{-2},4 x 10^{13} cm^{-2}.The

results are tabulated in Table 3. The cross-section of the devices after N_{RESURF} layer implants are shown in Fig. 5

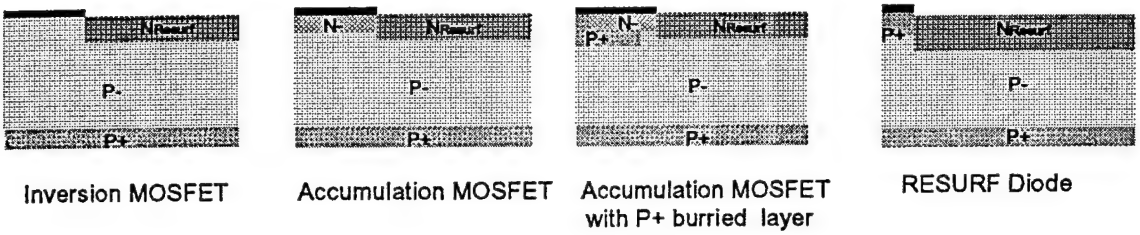


Figure 5. **Cross-section of the devices after RESURF layer implants.**

The sixth mask level is used to make N+ source and drain implants on the wafer. The oxide of thickness 0.85 μm was deposited in LPCVD system. The PECVD system can not be used for oxide deposition because of the technical problems. However, LPCVD system ,which is used for oxide deposition on vertically placed 4' and 6' wafers ,was calibrated with numerous test runs for the oxide deposition on horizontally placed 1.375 ' wafers. The best possible deviation obtained for oxide deposited oxide thickness was 3.5%. This was achieved by the mixture of O_2 at 210 sccm, and LTO at 87 sccm at 410 °C ,750 mTorr .The same procedure was used later in the process. The oxide was patterned using similar procedure as described for previous steps, using mask 6. After opening windows for source and drain layer implants, the wafers were sent for the multiple low energy Nitrogen ion implants at 1000 °C ,energy and dose combination of 40 keV ,8 x 10^{14} $cm^{-2}$and 100 keV , 8 x 10^{14} cm^{-2}; and a 0° tilt .The cross-section of the devices after source and drain implants are shown in Fig. 6

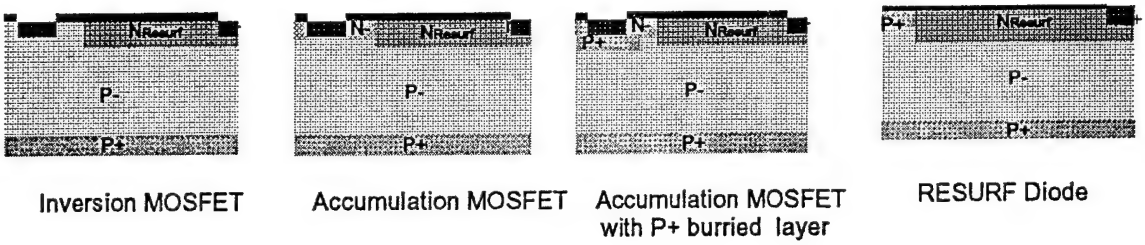


Figure 6. **Cross-section of the device after Source and Drain implants**

After the implants ,the PR was stripped and the oxide was removed with a blanket etch using BOE. The wafers were then cleaned using a standard RCA clean. The implants were given high temperature proximity-anneal at 1650 °C for 30 min. The proximity-anneal is done by capping the process wafer with another silicon carbide wafer, and placing both in SiC crucible. This is done to provide sufficient silicon carbide over-pressure to prevent the formation of pits by decomposition of silicon carbide at high temperatures. For the anneal, the furnace was ramped up at 5 °C/min from

room temperature to 1650 °C and then ramped down at 3 °C/min in an argon ambient. In the first run ,because of broken alumina furnace tube, the SiC crucible and two SiC wafers were oxidized . Also some surface damage in the form of pits was observed. However for the second run the alumina tube was replaced and the wafers were annealed without oxidation.

The seventh mask is used to open windows for gate oxide deposition .This is done by depositing oxide of thickness 1 μm and then patterning it using seventh mask. The procedure adopted here for opening windows for gate oxide deposition is similar to that adopted in previous masking steps. The gate oxide of thickness 500 A° was deposited in LPCVD system. The gate oxide was covered by thick amorphous silicon layer. This was achieved by depositing the 0.5 μm amorphous silicon in LPCVD system by the mixture of Disilane (Si_2H_6) at 50 sccm, 630 °C and 197 mTorr for 80 minutes. The amorphous silicon film was crystallized to polysilicon and doped by phosphorous disks at 900 °C for 60 minutes in a nitrogen ambient. Next the wafers were dipped in P-deglaze solution for 30 seconds to remove the phosphosilicate glass formed on the polysilicon layer during diffusion. Because of the process difficulties the sheet resistance of doped Poly-silicon layer couldn't be improved below 300 ohm/square. The cross-section of the devices after gate oxide deposition are shown in Fig. 7

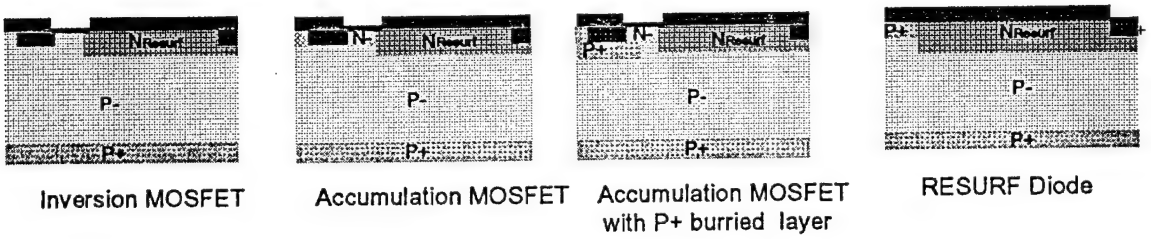


Figure 7. **Cross-section of the devices after Gate oxide-deposition**

The polysilicon was patterned using mask eight to define gate. Polysilicon was etched using the mixture of oxygen (O_2) at 55 sccm ,sulfur hexafluoride (SF_6) at 15 sccm ,at 60 mTorr and at the power of 100 W for 30 minutes. A 1.3 μm thick Photoresist was used as the mask during RIE. The oxide was etched by RIE to the depth of 0.8 μm and the rest by BOE. The cross-section of the devices after Poly-gate definition are shown in Fig. 8

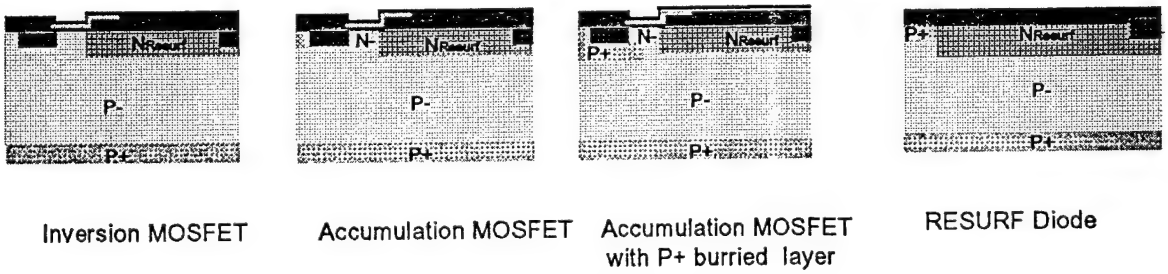


Figure 8. **Cross-section of the devices after Poly-gate definition.**

After stripping the photoresist,0.8 μm thick poly-isolation oxide was deposited on polysilicon in LPCVD. The contact areas were patterned using the ninth (Contact) mask level. The oxide was etched from the contact regions by RIE using the mixture of CHF_3 (25 sccm) and Argon (25 sccm) at 100 W,60 mTorr and 20 °C ,for 10 minutes. Any remaining oxide was removed using BOE. The cross-section of the devices after opening contact holes are shown in Fig. 9

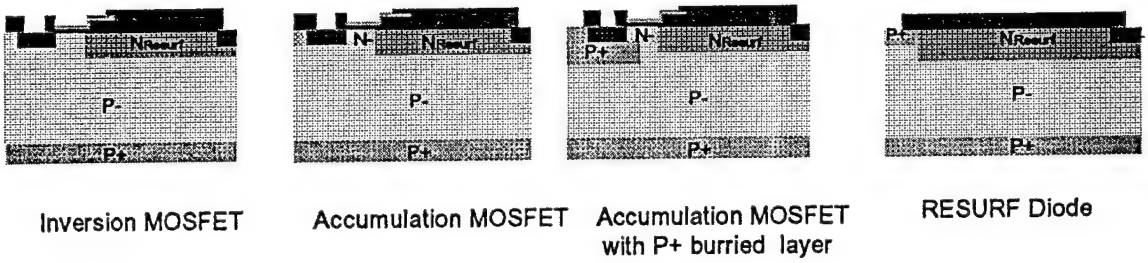


Figure 9. **Cross-section of devices after opening contact holes.**

The contacts to the P+ regions were made with aluminum by a lift-off process using the tenth mask level. The photoresist solution for the lift-off process was prepared by mixing 1.5 grams of Imidazole in 50 ml. of Shipley 1813 photoresist on a magnetic stirrer for 30 minutes. The solution was allowed to stand for 24 hours before use. The PR mixture was spun on the wafers at 3500 rpm for 40 seconds .After a bake at 90 C for 1 minute, the wafers were exposed to ultraviolet light in a Karl Suss MBJ3 aligner for 36 seconds at an intensity of 15 mW/cm^2. After exposure ,the wafers were baked at 115 °C for 75 seconds ,and were given flood exposure for 2.5 minutes. The photoresist was then developed for 40 seconds. Prior to metal deposition, any remnants of the photoresist in the developed areas were removed using lift-off descum procedure in Asher, which used oxygen plasma at 600 mTorr and 300 W to burn off photoresist at room temperature. 3000 A° of Aluminum was deposited on the wafers by electron beam deposition .The contact resistance of aluminum contacts was improved by annealing the wafers in forming gas ambient for 15 minutes at 700 °C. The cross-section of the devices after making aluminum contacts are shown in Fig. 10

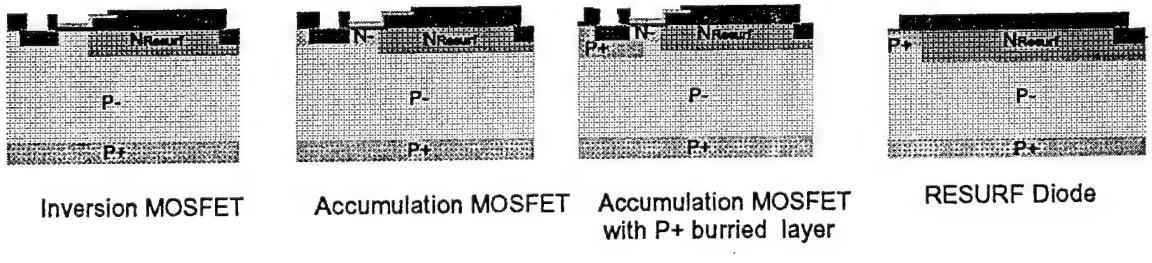


Figure 10. **Cross-section of the devices after making aluminum contacts.**

The polysilicon and oxide on the backside of the wafers was etched by RIE process using their respective etch recipes. The contacts to N+ regions were made with titanium by a lift-off process using the eleventh mask level as described in the following . Before spinning the photoresist ,the wafers were degreased with acetone and methanol, rinsed with DI water, dried with nitrogen and baked for 5 minutes at 115 °C . After the photoresist was patterned for lift-off as described above, approximately 2000 A° of titanium was deposited using e-beam deposition. The contact resistance of Titanium contacts was improved by annealing the wafers with forming gas ambient for 10 minutes at 500 °C. The cross-section of the devices after making titanium contacts are shown in Fig. 11

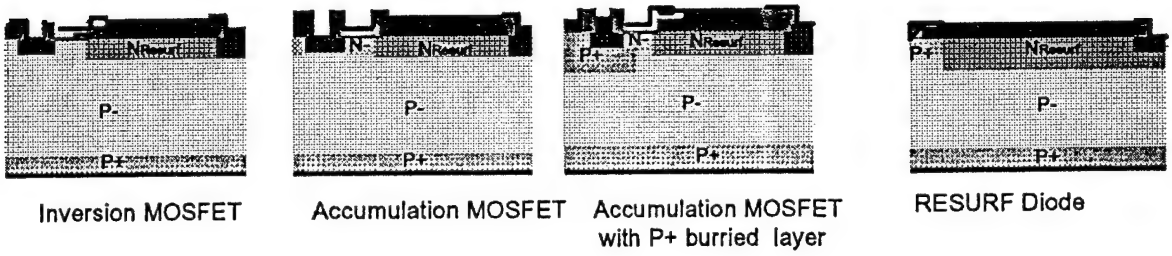


Figure 11. **Cross-section of devices after making titanium contacts .**

In the entire process utmost care was taken to ensure proper lithography ,oxide and Poly deposition and etching by RIE as well as BOE. This was ensured by carrying out many process simulation using process simulator SUPREM-IV and by test runs on monitor wafers. Also before dopant implants and metallization steps, care was taken that there are no residual photoresist in the implants/contact windows by removing it in Asher.

ACKNOWLEDGEMENT

The authors wish to thank the sponsors of the Power Semiconductor Research Center for supporting this research ,TMA for providing MEDICI device simulator, and Avanti Software for providing LTL layout tool.

REFERENCES

[1] R. Chilukuri and Dr. B.J Baliga, "High Voltage 4H-SiC ACCUFETs", Ph.D. dissertation 2000.
[2] S.Sridevan and Dr. B.J. Baliga, "Characterization of Inversion Layers in SiC," Ph.D. dissertation 1998.
[3] S.M. Sze , "VLSI Technology", McGraw-Hill Book Company, 1988.

Table 1: Mask Levels used for LATERAL RESURF MOSFETs and Diodes process run

Mask Level	Mask Name	Mask Type	Photoresist	Alignment to level
1	Align Mark	Dark Field	Positive	-
2	P+ Burried	Dark Field	Positive	1
3	P+ Sinker	Dark Field	Positive	1
4	N- Layer	Dark Field	Positive	1
5	N_{RESURF}	Dark Filed	Positive	1
6	N+ Source/Drain	Dark Filed	Positive	1
7	Gate Oxide	Dark Field	Positive	1
8	Poly Gate	Light Field	Positive	1
9	Contact	Dark Field	Positive	8
10	Aluminum contact	Light filed	Negative	9
11	Titanium Contact	Light filed	Negative	10

Table 2: Wafer-split ion implantation details

Wafer No.	Implant Energy in 1st Half of SiC Wafer	Dose in 1st Half of SiC Wafer	Implant Energy in 2nd Half of SiC Wafer	Dose in 2nd Half of SiC Wafer
1	250 keV	1×10^{12} cm^{-2}	250 keV	2×10^{12} cm^{-2}
2	250 keV	3×10^{12} cm^{-2}	250 keV	6×10^{12} cm^{-2}
3	250 keV	8×10^{12} cm^{-2}	250 keV	1.6×10^{13} cm^{-2}
4	250 keV	2×10^{13} cm^{-2}	250 keV	4×10^{13} cm^{-2}

Table 3: LATERAL RESURF MOSFET process flow

Step #	Step	At	Tool	Wafer Description	# of wafers
1	**Label Wafers:** 4 4H-SiC (1,2,3,4) **Label 1.5 inch silicon monitor wafers:** m1-m10				
2	**JT Baker Clean** JT Baker solution 5min; DI rinse 5 min Blow Dry; Bake 115C for 5 min	AEMP	JTB clean hood	1-4	4
3	**Alignment Marks - Mask 1 Dark Field** Dry Wafers 5 min at 115C Spin PR @ 4500 rpm for 40 secs Pre Expose Bake for 1 min @ 90C Shoot Wafers on Contact Karl-Suss Jr (MJB3) Aligner (Mask 1: Alignment Marks) Post expose bake for 1 min at 115C Developer 1 min, DI rinse 5 min, blow dry Post develop bake for 1 min at 90C **Check feature size. If not OK, repeat with different exposure time**	AEMP	Karl-Suss MBJ3 Aligner	1-4	4
4	**SiC Reactive Ion Etching**: ***Recipe 1***: (SF_6 = 9sccm; O_2 = 1 sccm; Time = 8min; Power = 120W; Pressure = 15mTorr; Temp= 15C) Depth=0.25-0.3 microns	PSRC	Oxford RIE	1-4	4
5	Strip PR using Nanostrip and Asher	AEMP	March Instr	1-4	4
6	JT Baker Clean (see step 2)	AEMP	JTB Clean hood	1-4; m1	5
7	**Oxide Deposition - LTO Process** PECVD, Oxide thickness = 1.5 microns ***Recipe 2***: (N_20 = 710 sccm; SiH_4(in He) =170sccm; Power = 20 W; Pressure = 1mTorr; Temp =300 °C; Time = 75 min) **Note: Load Wafers at room temp. Verify thickness using Filmetrics**	PSRC	PECVD	1-4,m1	5
8	**P+ Buried Implant - Mask 2 DF** Follow Step 3 Process **(Mask 2: Layer 2 - align with layer 1)** **Check Feature size. If not OK repeat with different exposure time**	AEMP	Karl-Suss MBJ3 Aligner	1-4,m1	5
9	**OxideEtch:** RIE etch oxide - remove approx 1.3 microns ***Recipe 3:***CHF_3 =25 sccm; Ar =25 sccm ;Time =45 min ;Power =100 W ;Pressure=60mTorr; Temp=20 °C) Bake at 115C for 5 min BOE etch remaining oxide Stop BOE etch every 5 min; repeat post-develop bake; continue etch.(Check etch rate with m1)	PSRC, AEMP	RIE, BOE - Hood	1-4,m1	5

Step #	Step	At	Tool	Wafer Description	# of Wafers
10	Strip PR using nanostrip and Asher	AEMP	March Instr	1-4	4
11	JT Baker Clean	AEMP	JTB Clean Hood	1-4	4
12	**Boron Ion Implant:** Send to Implant Science Boron Dose = 1e14 /cm^2; Energy = 380keV Temperature = 1000C ; Angle = 0 degrees **Implant on Front side of wafers**	Implant Science	Vendor Locn.	1-4	4
13	**Blanket etch oxide:** BOE	AEMP	BOE - Hood	1-4	4
14	JT Baker Clean	AEMP	JTB clean Hood	1-4, m2	5
15	**Oxide Deposition - LTO Process (Recipe 2)** PECVD, Oxide thickness = 1 microns **Note: Load Wafers at room temp. Verify thickness using Filmetrics**	AEMP	PECVD	1-4,m2	5
16	**P+ Sinker Implant - Mask 3 DF** Follow Step 3 Process **(Mask 3: Layer 3 - align with layer 1)** **Check Feature size. If not OK, repeat with different exposure time**	AEMP	Karl-Suss MBJ3 Aligner	1-4,m2	5
17	**OxideEtch:** BOE etch oxide Stop BOE etch every 5 min; repeat post-develop bake; continue etch Check etch rate using monitor wafer m2.	AEMP	BOE - Hood	1-4,m2	5
18	Strip PR using nanostrip and Asher	AEMP	March Instr	1-4	5
19	JT Baker Clean	AEMP	JTB clean hood	1-4	5
20	**Aluminium Ion Implant:** Send to Implant Science Al Dose = 1e15/cm^2 ; Energy = 25keV Al Dose = 1e14/cm^2 ; Energy = 75keV Al Dose = 1e14/cm^2 ; Energy = 250keV Temperature = 1000C ; Angle = 0 degrees **Implant on Front side of wafers**	Implant Science	Vendor Locn.	1-4	5
21	**Blanket etch oxide:** BOE	AEMP	BOE - Hood	1-4	5
22	JT Baker Clean	AEMP	JTB clean hood	1-4, m3	5
23	**Oxide Deposition - LTO Process (Recipe 2)** PECVD, Oxide thickness = 1 micron **Note: Load Wafers at room temp. Verify thickness using Filmetrics**	AEMP	PECVD	1-4,m3	5
24	**N- Implant: Mask 4 DF** Follow Step 3 Process **(Mask 4: Layer 4 - align with layer 1)** **Check Feature size. If not OK, repeat with different exposure time**	AEMP	Karl-Suss MBJ3 Aligner	1-4,m3	5

Step #	Step	At	Tool	Wafer Description	# of Wafers
25	**OxideEtch:** RIE etch oxide (Recipe 3) - remove approx. 0.8μ Bake at 115C for 5 min BOE etch remaining oxide Stop BOE etch every 5 min; repeat post-develop bake; continue etch Check etch rate using monitor wafer m3.	PSRC, AEMP	RIE, BOE - Hood	1-4,m3	5
26	Strip PR using nanostrip and Asher	AEMP	March Instr	1-4	5
27	JT Baker Clean	AEMP	JTB clean hood	1-4	5
28	**Nitrogen Ion Implant:** Send to Implant Science Dose = 5e11/cm^2 ; Energy = 150keV Temperature =1000C ; Angle = 0 degrees **Implant on Front side of wafers**	Implant Science	Vendor Locn.	1-4	5
29	**Blanket etch oxide:** BOE	AEMP	BOE - Hood	1-4	5
30	JT Baker Clean	AEMP	JTB clean hood	1-4, m4	5
31	**Oxide Deposition - LTO Process (Recipe 2)** PECVD, Oxide thickness = 1 micron **Note: Load Wafers at room temp. Verify thickness using Filmetrics**	AEMP	PECVD	1-4,m4	5
32	**N RESURF Implant: Mask 5 DF** Follow Step 3 Process **(Mask 4: Layer 4 - align with layer 1)** **Check Feature size. If not OK, repeat with different exposure time**	AEMP	Karl-Suss MBJ3 Aligner	1-4,m4	5
33	**OxideEtch:** RIE etch oxide (Recipe 3) - remove approx 0.8 μ Bake at 115C for 5 min BOE etch remaining oxide Stop BOE etch every 5 min; repeat post-develop bake; continue etch Check etch rate using monitor wafer m4.	PSRC, AEMP	RIE, BOE - Hood	1-4,m4	5
34	Strip PR using nanostrip and Asher	AEMP	March Instr	1-4	4
35	JT Baker Clean	AEMP	JTB clean hood	1-4	4
36	**Nitrogen Ion Implant:** Send to Implant Science Process split involved here - one half of each wafer gets a different implant. Doses decided were 1e12-2e12; 3e12-6e12; 8e12-1.6e13; 2e13-4e13 /cm^2 . Energy = 250keV (and possibly 40keV @ $1/10^{th}$ dose to get a more uniform profile) Temperature = 1000C ; Angle = 0 degrees **Implant on Front side of wafers**	Implant Science	Vendor Locn.	1-4	4
37	**Blanket etch oxide:** BOE	AEMP	BOE - Hood	1-4	4
38	JT Baker Clean	AEMP	JTB - Hood	1-4, m5	5

Step #	Step	At	Tool	Wafer Description	# of Wafers
39	**Oxide Deposition - LTO Process** LPCVD, Oxide thickness = 0.8 microns *Recipe 4*: (O_2 =210 sccm, LTO =87 sccm , Temp =410 C, Press = 750 mTorr, Time = 55 min) **Note: Load Wafers at room temp. Verify thickness using Filmetrics**	AEMP	LPCVD	1-4,m5	5
40	**N+ Src/Drain Implant: Mask 6 DF** Follow Step 3 Process **(Mask 6: Layer 7 - align with layer 1)** **Check Feature size. If not OK, repeat with different exposure time**	AEMP	Karl-Suss MBJ3 Aligner	1-4,m5	5
41	**OxideEtch:** RIE etch oxide (Recipe 3) - remove approx 0.6 μ Bake at 115C for 5 min BOE etch remaining oxide Stop BOE etch every 5 min; repeat post-develop bake; continue etch Check etch rate using monitor wafer m5.	AEMP	RIE, BOE -Hood	1-4,m5	5
42	Strip PR using nanostrip and Asher	AEMP	March Instr	1-4	4
43	JT Baker Clean	AEMP	JTB clean hood	1-4	4
44	**Nitrogen Ion Implant:** Send to Implant Science Dose = 8e14/cm^2 ; Energy = 40, 100keV Temperature =1000C ; Angle = 0 degrees **Implant on Front side of wafers**	Implant Science	Vendor Locn.	1-4	4
45	**Blanket etch oxide:** BOE	AEMP	BOE - Hood	1-4	4
46	JT Baker Clean	AEMP	JTB clean Hood	1-4	4
47	**Ion Implant Annealing** Use SiC crucible with SiC capping wafer Ar ambient; T=1650C; Time=30min; Ramp up @ 3C/min; Ramp down @ 5C/min	PSRC	1700C Furnace	1-4	4
48	RCA Clean	AEMP	RCA clean hood	1-4,m6	5
49	**Deposit Field Oxide: LTO Process (Recipe 4)** PECVD, Oxide Thickness = 1 micron	AEMP	LPCVD	1-4;m6	5
50	**Gate Oxide Region: Mask 7 DF** Follow Step 3 Process **(Mask 7: Layer 8-align with layer 1)** **Check Feature size. If not OK, repeat with different exposure time**	AEMP	Karl-Suss MBJ3 Aligner	1-4,m6	5
51	**Oxide Etch:** RIE etch oxide (Recipe 3) - remove approx 0.8 μ Bake at 115C for 5 min BOE etch remaining oxide Stop BOE etch every 5 min; repeat post-develop bake; continue etch Check etch rate using monitor wafer m6.	AEMP	RIE	1-4,m6	5

Step #	Step	At	Tool	Wafer Description	# of Wafers
52	Strip PR using nanostrip and Asher	AEMP	March Inst.	1-4	4
53	**Gate Oxide Deposition - LTO Process** LPCVD, Oxide thickness = 500A **Note: Load Wafers at room temp. Verify thickness using Filmetrics. Monitor thickness with m7**	AEMP	LPCVD	1-4	4
54	**Poly Deposition** Thickness = 5000A *Recipe 5:* (Si_2H_6 = 50sccm; Temp=630C, Pressure=197mTorr,Time =80 min.) Verify thickness using Filmetrics	AEMP	LPCVD	1-4,m7	5
55	**Phosphorous diffusion of Poly** 900C for 60 min	AEMP	P-diffusion furnace	1-4,m7	5
56	**P-Deglaze**	AEMP	P -Deglaze hood	1-4	4
57	**Gate definition: Mask 8 LF** Follow Step 3 Process **(Mask 8: Layer 9- align with layer 8)** **Check Feature size. If not OK, repeat with different exposure time**	AEMP	Karl-Suss MBJ3 Aligner	1-4,m7	5
58	**Poly Etch (RIE) : Thickness = 5000 A** **Recipe 6:** (O_2 = 55 sccm, SF_6 =15 sccm, Power =100W, Pressure = 60 mTorr, Time = 30 min) **Oxide Etch** RIE: Thickness = 0.8μ ,Recipe 3 Bake at 115C for 5 min BOE etch remaining oxide Stop BOE etch every 5 min; repeat post-develop bake; continue etch Check etch rates using monitor wafer m7.	AEMP	RIE	1-4,m7	5
59	Strip PR using nanostrip and Asher	AEMP	March Inst.	1-4	4
60	**Oxide Deposition :LTO Process (Recipe 4)** Oxide Thickness = 0.8 micron Monitor thickness with m8	AEMP	PECVD	1-4,m8	5
62	**Contact Windows: Mask 9 DF** Follow Step 3 Process **(Mask 9: Layer 10-align with layer 9)** **Check Feature size. If not OK, repeat with different exposure time**	AEMP	Karl-Suss MBJ3 Aligner	1-4,m8	5
63	**Oxide Etch:** **Oxide Etch** RIE: Thickness = 0.6μ ,Recipe 3 Bake at 115C for 5 min BOE etch remaining oxide Stop BOE etch every 5 min; repeat post-develop bake; continue etch Check etch rates using monitor wafer m8	AEMP	RIE	1-4,m8	5
64	Strip PR using nanostrip and Asher	AEMP	March Inst.	1-4	5
65	Huang/RCA Clean	AEMP	RCA Hood	1-4,m9	5

Step #	Step	At	Tools	Wafer Description	#of Wafers
66	**Metal 1 (Aluminum): Mask 10 LF** Lift Off Process **(Mask 10: Layer 11-align with layer 10)** **Check Feature size. If not OK, repeat with different exposure time**	AEMP	Karl-Suss MBJ3 Aligner	1-4,m9	5
67	Liftoff descum in Asher	AEMP	March Inst.	1-4m9	5
68	Aluminium Evaporation (e-beam evaporation) Thickness = 3000 A Check thickness using monitor wafer m9 and Dektak Proflimeter	AEMP	e-Beam Evaporation System	1-4,m9	5
69	Lift Off Process Leave Wafers in lift of solution for several hours/overnight	AEMP	Developer Hood	1-4,m9	5
70	Aluminium Contact Annealing Temp = 700C , Forming Gas , Time = 15 min.	AEMP	Annealing Furnace	1-4	4
71	Liftoff descum in Asher	AEMP	March Inst.	1-4	4
72	**Metal 2 (Titanium): Mask 11 LF** Lift Off Process **(Mask 11: Layer 11-align with layer 10)** **Check Feature size. If not OK, repeat with different exposure time**	AEMP	Karl-Suss MBJ3 Aligner	1-4,m10	5
73	Liftoff descum in Asher	AEMP	March Inst.	1-4,m10	5
74	Titanium Evaporation - (e-Beam Evaporation) Thickness = 5000 A Check thickness using monitor wafer m10 and Dektak Proflimeter	AEMP	e-Beam Evaporating System	1-4,m10	5
75	Lift Off Process (Details: from Ravi) Leave Wafers in lift of solution for several hours/overnight	AEMP	Developer Hood	1-4,m10	5
76	Liftoff descum in Asher	AEMP	March Inst.	1-4	4
78	Titanium Contact Annealing Temp = 500 C, Forming Gas, Time= 10 min	AEMP	Annealing furnace	1-4	4
77	Device Testing	PSRC	Test Lab	1-4	4

A Novel Device Isolation Technology for 4H-SiC

P. R. Singh, S. Venkatesan and B. J. Baliga
Power Semiconductor Research Center
North Carolina State University
Raleigh NC 27695, USA
Phone: (919)-515-6175 Fax: (919)-515-6170

Abstract

The vertical channel structure is more suitable for a power device. At the same time lateral devices offer simplicity in fabrication. So to optimize a Power IC, it will be good to have both, vertical and lateral devices. In the present work, it is demonstrated that vertical as well as lateral devices can be fabricated in an IC. Through simulations that it is shown that ion implanted layer can provide vertical isolation. It is also shown that the 4H-SiC lateral N-channel MOSFETs and P-channel MOSFETs can be fabricated in the thin active SiC layer formed on top of a high resistivity isolation layer provided the layer is sufficiently deep. Vertical isolation at the required depth can be provided by ion implantation of light species ion, Hydrogen and Helium. To study the viability of isolation, Schottky diodes with implanted layer, are fabricated and the characteristics are evaluated. For Hydrogen implanted diodes the isolation is found to be working up to 50-150 V. Reverse breakdown voltage of these devices are 1400-1700V. These diodes are also used for finding the trap level using Deep Level Transient Spectroscopy (DLTS).

I. Introduction

In power semiconductor devices vertical device structure is preferred. The vertical channel structure is more suitable for a power device because of higher device density and because of reduction in the electric field crowding in the device. At the same time lateral devices offer simplicity in fabrication. So to optimize a Power IC, it will be good to have both, vertical and lateral devices. One of the example of IC with vertical and lateral devices is shown in fig. 1. In the figure a N-channel MOSFET is shown with a Dual-channel MOSFET. We have not come across any work on integration of vertical and lateral devices in SiC. There is lot of work done for lateral isolation in SiC. Some work has also been reported on the vertical isolation. Some of work on vertical isolation include SIMOX[1], wafer bonding[2], and through ion implantation. In ion implantation work has been reported using vanadium[3] and hydrogen[4] ions. For vertical isolation in the IC, only the ion implantation technique can be used as selected area implant can be done. It is known that the defects generated by ion implantation produce deep level traps. The Deep level traps capture the carriers and hence high resistivity in the semiconductor.

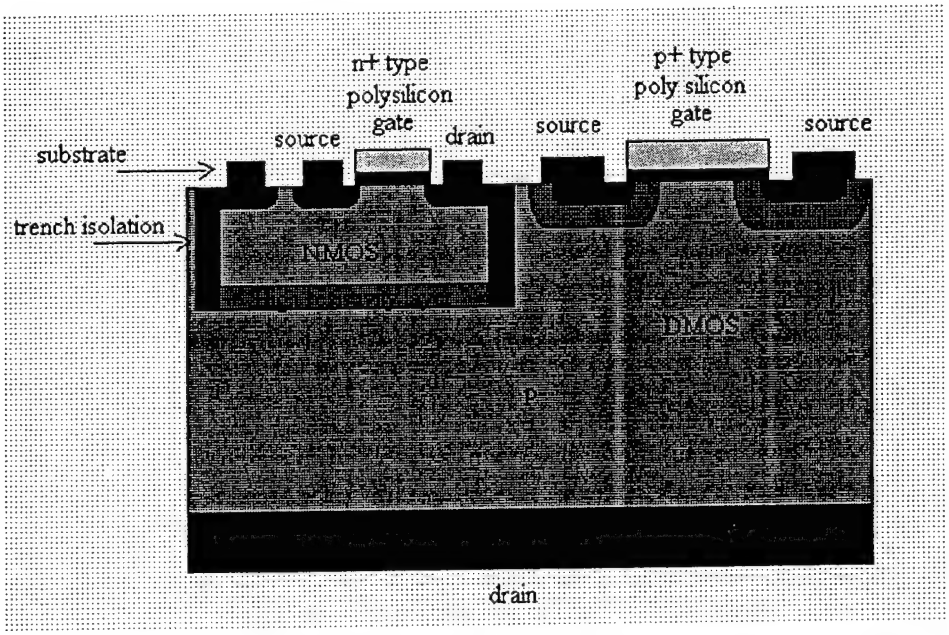


Fig. 1. Example of a IC with vertical and lateral devices

In the present research work, it is demonstrated that the 4H-SiC lateral N-channel MOSFETs and P-channel MOSFETs can be fabricated in the thin active SiC layer formed on top of a high resistivity isolation layer. The isolation layer is formed by ion implantation of light neutral ions, such as hydrogen and helium to produce deep level traps. To study the viability of isolation, Schottky diodes with implanted layer, are fabricated and the characteristics is evaluated using the I-V plot. These diodes are also used for finding the trap level using Deep Level Transient Spectroscopy (DLTS).

II. Simulations

A. Initial simulations

Extensive 2-dimensional simulation were performed using MEDICI. Simulations were done to determine the resistivity change when a donor level trap is introduced at mid-gap. The resistivity , hole and electron concentration were determined with change in trap concentration. The concentration of the traps was changed over range 1e10 to 1e20 cm^{-3}. It is found that resistivity is maximum when the trap concentration is between 1e16 to 2e16 cm^{-3}. The maximum resistivity is found to be 1.05e22 ohm-cm at 1.5e16cm^{-3} trap concentration. This resistivity is high enough to provide isolation.

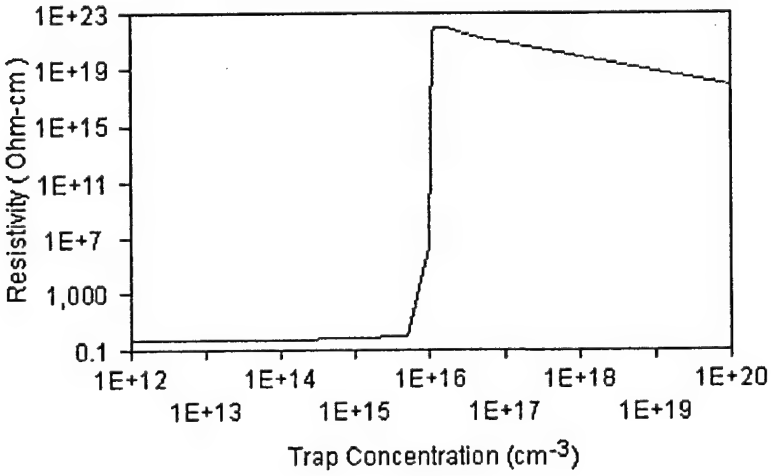


Fig.2 Resistivity vs trap concentration

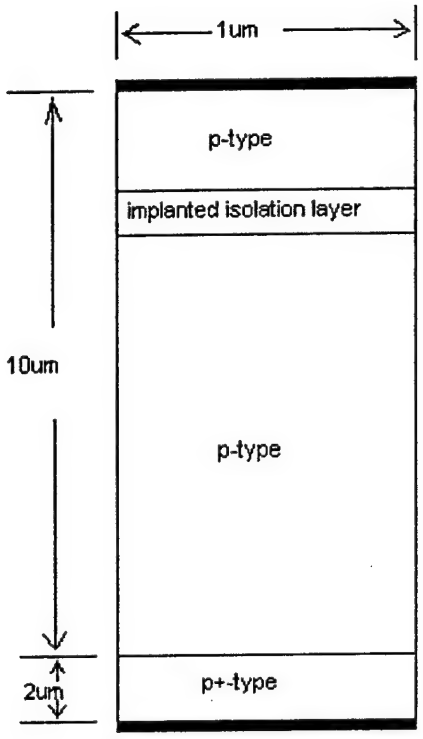


Fig. 3. Schottky diode structure

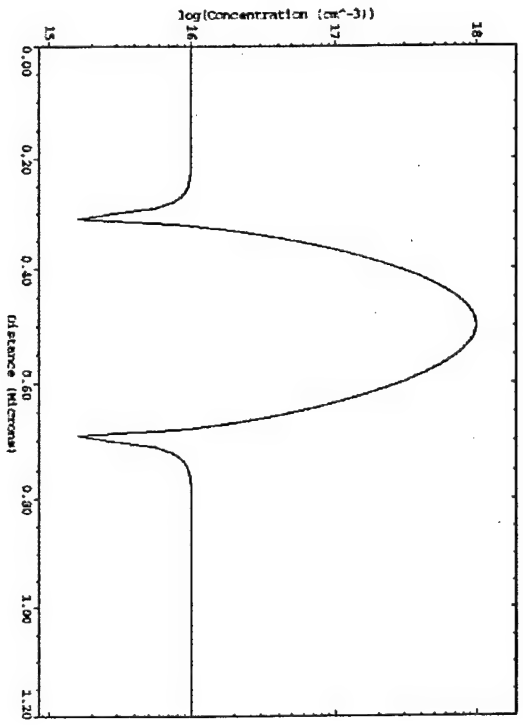


Fig. 4. Schottky diode doping profile

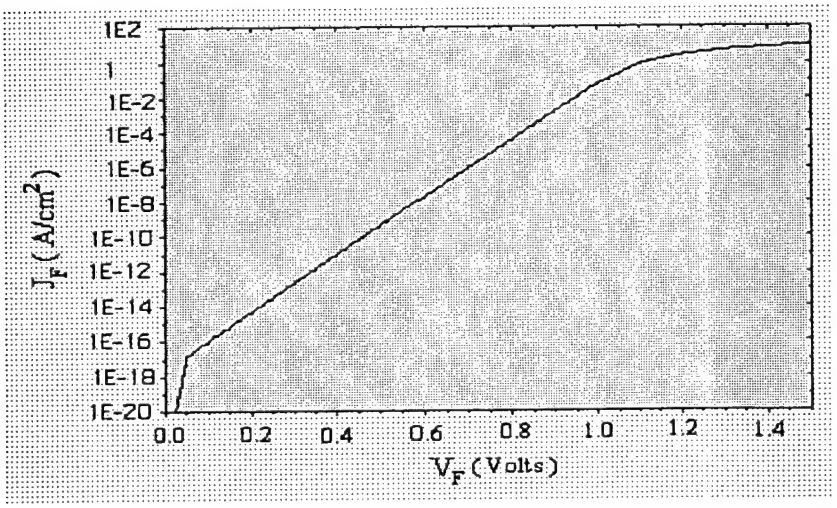
B. Schottky Diode Simulations

To study the properties of the high resistivity layer Schottky diodes with isolation layer are simulated. For the Schottky diode, the 4H-SiC epitaxial layer is p-type ($1x10^{16}$ cm^{-3}, aluminum doped) on p+ substrate and is 10 μm thick. The forward voltage drop of the Schottky diode is given by-

$$V_F = \frac{\eta k T}{q} \ln\left(\frac{J_F}{A^* T}\right) + \eta \Phi_{bn} + R_{s,sp} J_F$$

Where k is Boltzman's constant, η is ideality factor, J_F is current density, A^* is the effective Richardson's constant, Φ_{bn} is the barrier height, and $R_{s,sp}$ is the specific series resistance. The contact metal is defined to have barrier height of 1.4 eV as reported for 4H-SiC and Titanium/Aluminum contact [5]. The I-V plot of the Schottky diode is given in figure 5(a). To study the effect of deep level traps, donor type mid-gap material is inserted as given in figure 3 and figure 4. The profile of the traps is taken to be gaussian

as they are to be implanted. The characteristic length of the gaussian distribution is taken to be that of Helium implant. The simulations were performed for 0.5 μm to 1.5 μm depth of the peak trap concentration. To vary the thickness of the layer two trap profiles separated by small distance is simulated. The peak concentration of the traps is varied from 1e17 to 1e19 cm^{-3}. The I-V curves for a typical Schottky diode with isolation layer is given in figure 5(b). There is a shift in I-V from 10's of Volts to 100's of Volts depending upon the trap concentration and depth.



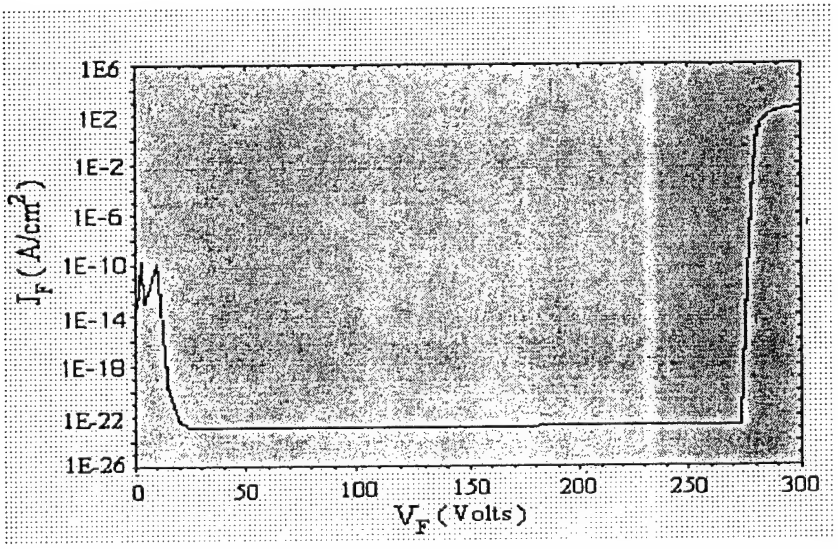


Fig. 5. J_F vs V_F for (a) Schottky diode (b) Schottky diode with isolation layer

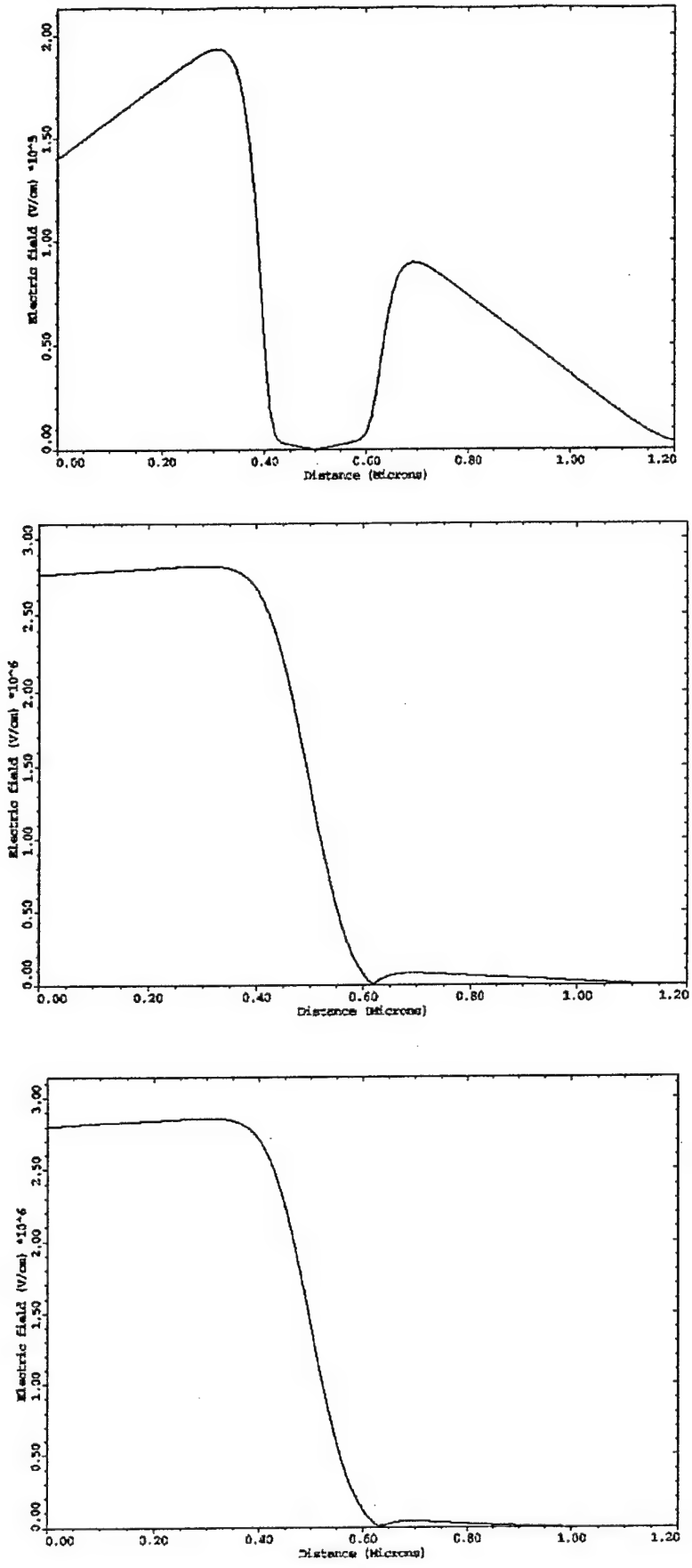


Fig. 6. E-field vs depth at (a) low voltage (b) before breakdown (c) after breakdown

The behavior of the implanted layers can be explained by examining the electric field distribution in the Schottky diodes. If the applied voltage is such that the Schottky junction is forward biased the most of the potential falls across the depletion region created between the implanted layer and the epilayer. In the figure 6, magnitude of the electric field vs. depth for single implant (Peak density = 1e18 at depth = 0.5 μm) and for forward biased Schottky are plotted. When applied voltage is low (Figure 6(a)) there is formation of depletion region at the junction between the epilayer and the implanted region. As the voltage is increased there is increase in the depletion width (Figure 6(b)). finally when the whole implanted layer is consumed the depletion can no longer increase and current start flowing (Figure 6(c)). For other implantation the same behavior is observed. Increase in peak concentration or multi-depth doping increases the supported voltage.

The simulation results imply that this layer can be used as isolation. As SiC devices are used for power applications , the simulation were performed up to 500 K and isolation is found to perform satisfactory.

C. MOS simulations

MEDICI simulations were performed to determine whether N-channel MOSFET and P-channel MOSFET can be fabricated on the top of such isolation layer. The structure used for N-channel MOSFET is given in figure 7. The gate length is 2μm, depth of source and drain is 0.1μm, gate thickness is 20nm. The isolation layer Peak concentration is 1e16 cm-3. The depth of the isolation layer is varied. Negative voltage is applied to the back contact of the NMOSFET to study the effect of the isolation layer. The Potential and electric field plot (Figure 8 , back contact potential = -100V, when other terminals are grounded) in the device shows that potential drop is across the isolation layer and the epilayer on the back contact side.

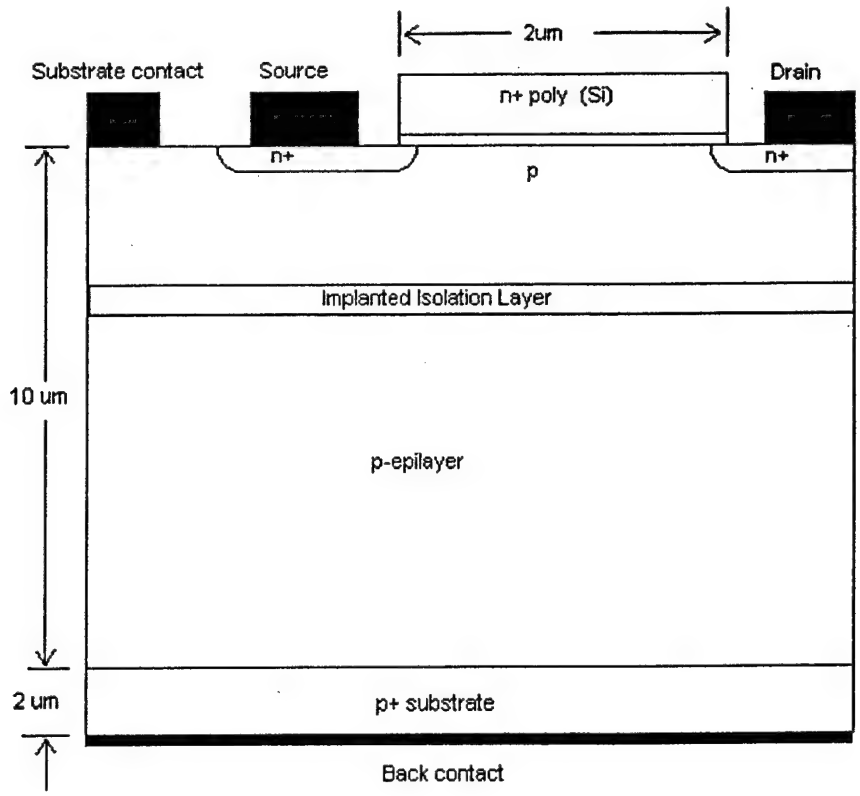


Fig. 7. Structure for N-channel MOSFET on top of the isolation layer

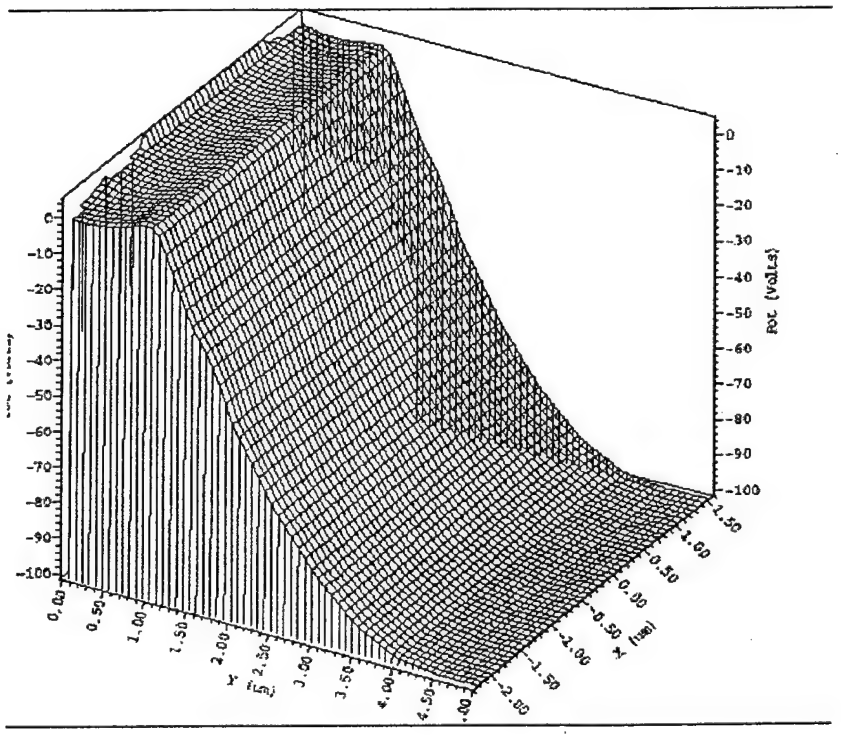


Fig. 8(a) Potential plot in the device at back contact potential of -100V

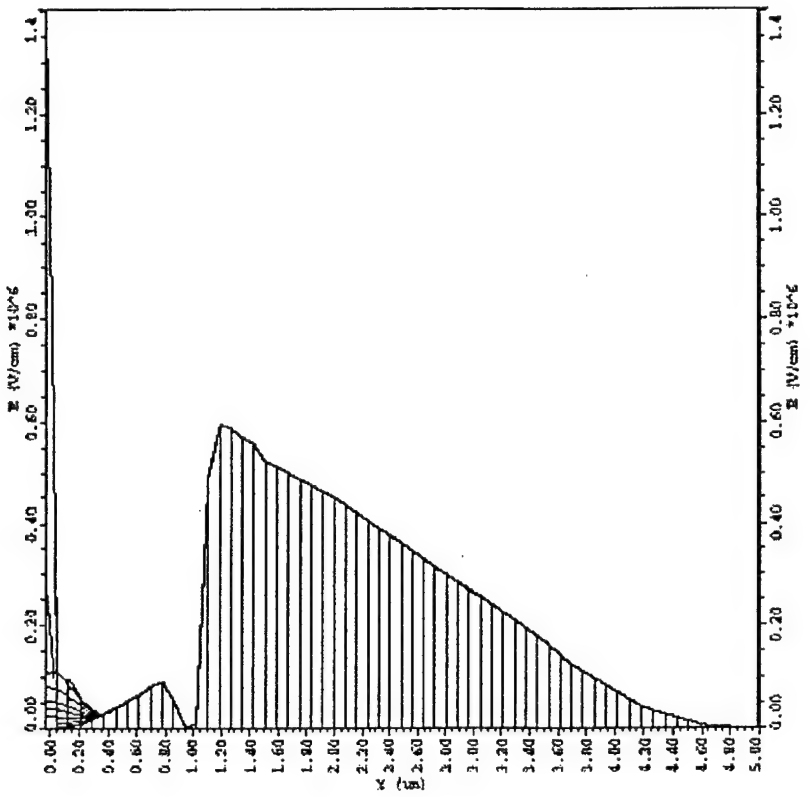


Fig. 8(b) Electric field in the device at back contact potential of -100V.

The depth of the isolation layer is not a factor when the isolation from the back contact is considered but it is found that if isolation layer is not sufficiently deep from the surface then it affects the operation of MOSFET. The current density plot (Figure 9) suggest that the current tend to flow though the isolation layer is it is close to source and drain. The Depth of the isolation layer is function of operating voltage of the device. For example, Ids vs Vds is for different depths is plotted at 5V gate voltage in the figure 10. The layer provide good isolation of the MOSFET from the back contact for at least up to 100V.

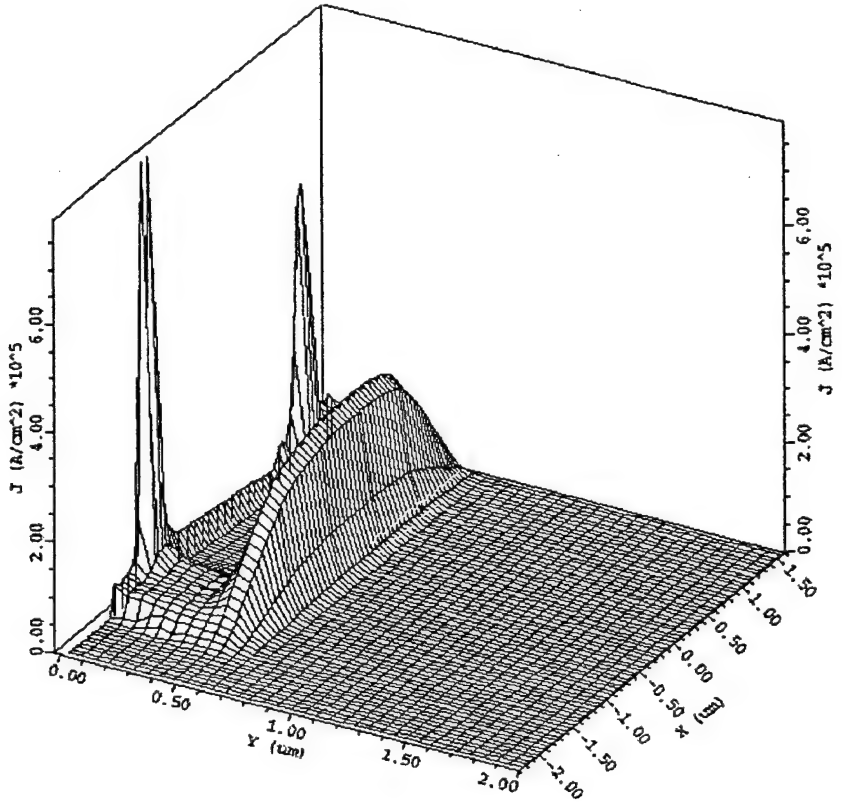


Fig. 9 Current density plot in the device with isolation layer peak at 0.5 μm (V_{GS} = 5V, V_{DS} = 5V)

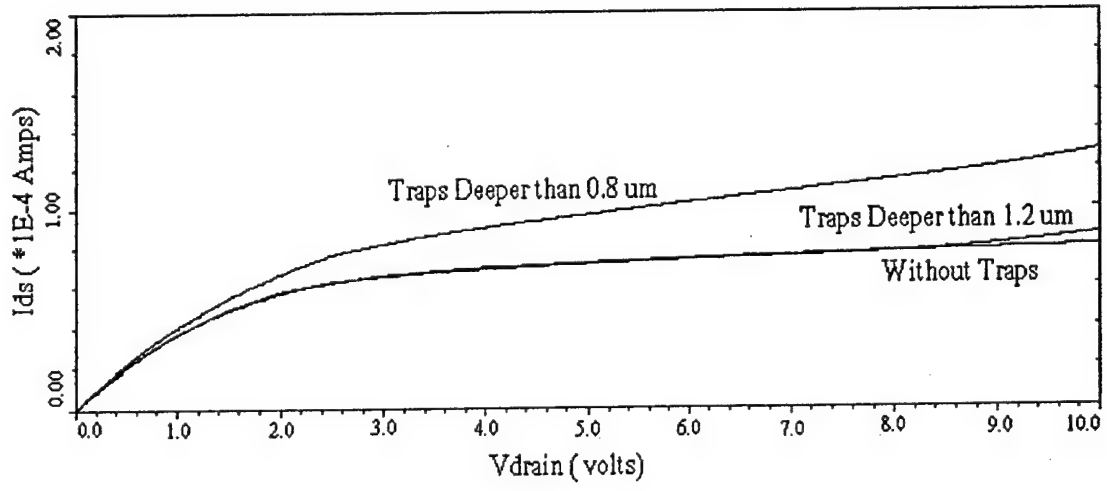


Fig. 10 Ids vs Vds at gate voltage of 5V.

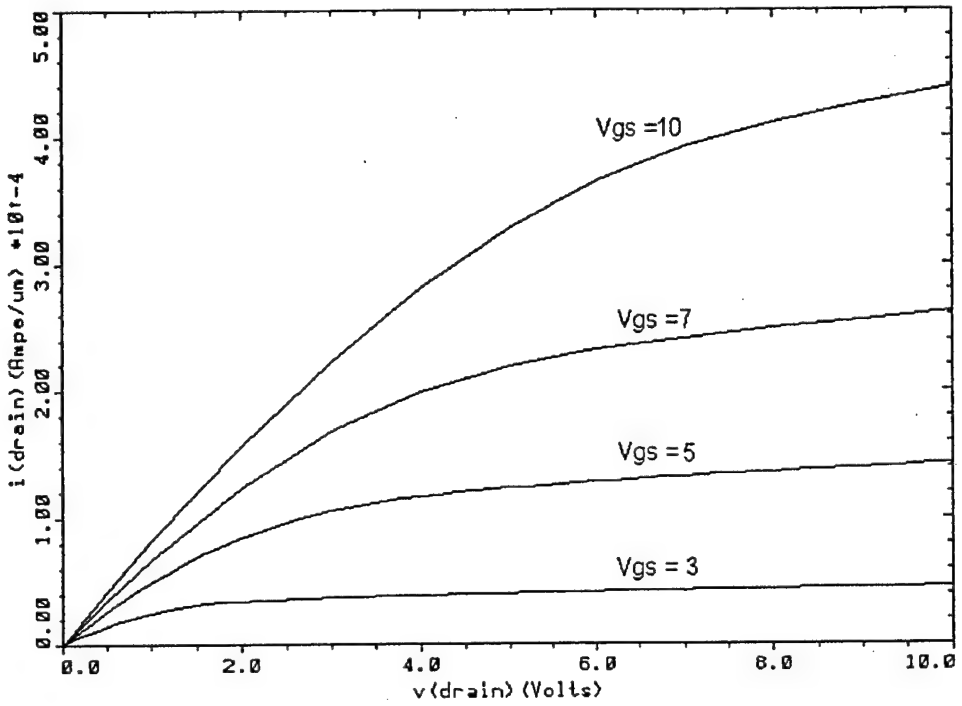


Fig. 11(a) IVs for NMOSFET without isolation layer

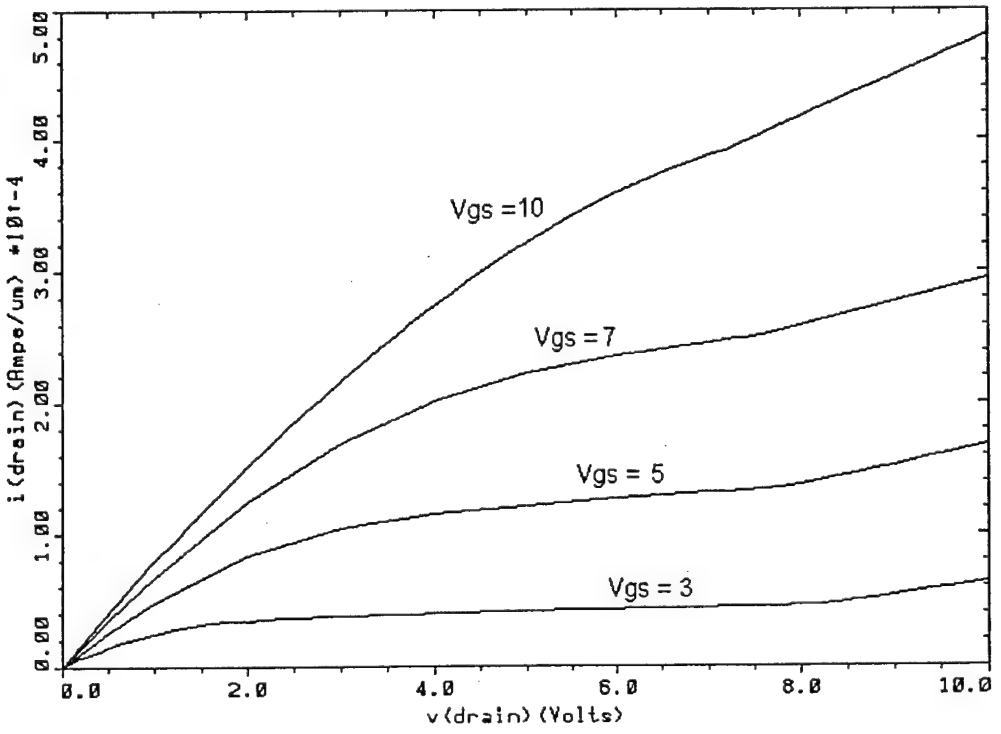


Fig. 11(b) IVs for NMOSFET with isolation layer deeper than 1.2 μm

For traps deeper than 1.2 μm , IVs of NMOSFET, with isolation layer, are identical to IVs of NMOSFET, without isolation layer, (figure 11) up to approximately 7V. For the same depth of implanted traps in PMOSFET, the IVs (figure 12) are not affected . This can be explained as the donor traps can be considered as a part of the well.

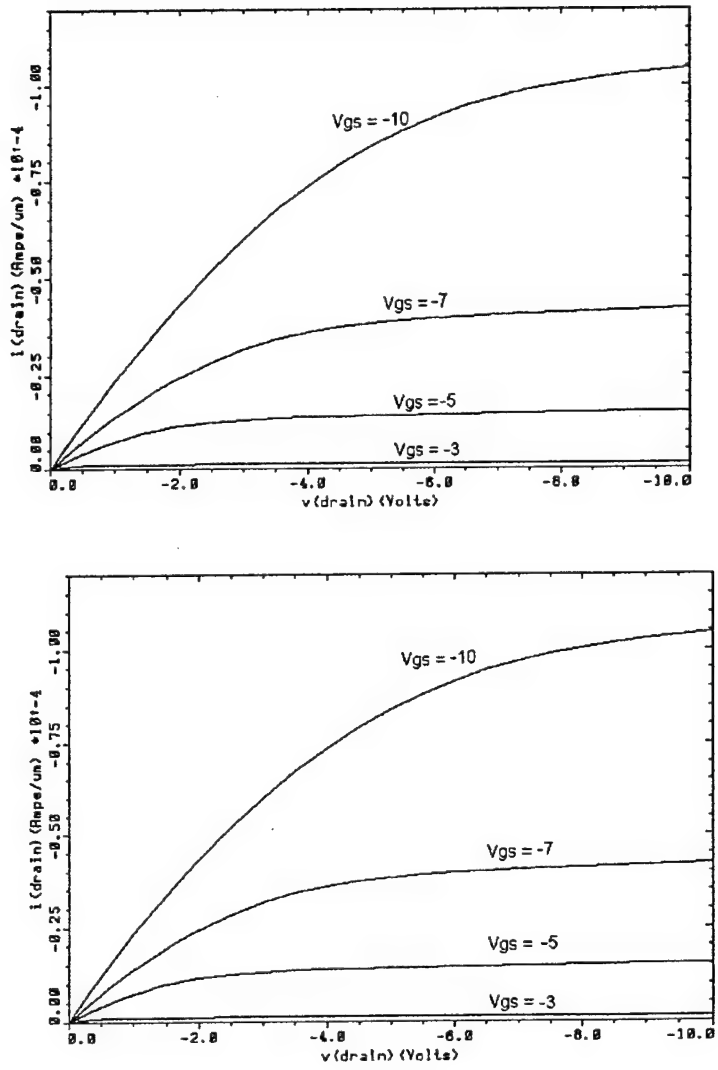


Fig. 12 IVs of PMOSFET (a) without isolation layer (b) with isolation layer deeper than 1.2μm

D. SUPREM simulations

TSUPREM4 simulations were performed to find the implantation energy, dose of the implant to form isolation layer. It is found that given the maximum energy of 200keV only lighter species, H^+ and He^+,can give required depth.

III. Device Fabrication

On the basis of simulations, Schottky diodes were fabricated with implanted layers. The four implantation are:

1. H^+ ion implantation at 200 keV with dose 1e15 cm^{-2},
2. H^+ ion implantation at 200 keV with dose 1e15 cm^{-2} and at 160 keV with dose 1e15 cm^{-2},
3. H^+ ion implantation at 200 keV with dose1e16 cm^{-2},
4. He^+ ion implantation at 200 keV with dose 1e16 cm^{-2}.

The after the implantation the wafer was given a RCA clean (10-min dip in $NH_4OH:H_2O_2:H_2O::1:1:6$ followed by a 10-min dip in $HCl:H_2O_2:H_2O::1:1:6$ solution at 75°C). Schottky diodes of diameter, 100μm and 350μm, were fabricated using shadow mask. First 1000 A° of contact metal Ti was deposited and on top of it 5000A° of Al was deposited. Al was deposited so that good contact for electrical probing can be formed. Blanket evaporation of Ti/Al was done on the heavily doped substrate to form a large area backside contact.

IV. Experimental results

A. IV characterization

The IV for Schottky diodes is given in fig.1. From the IV the following conclusions can be made. The hydrogen implanted layer can provide isolation up to 50-150V at room temperature and 50-100V at 400°K. The Helium implanted layer does not provide isolation. High slope of the curve is credited to the high resistance of the implanted layer. In the Fig.12, the reverse breakdown voltages (at 1 μA current) of the devices are given. The Hydrogen implanted Schottky have BV higher than 1400V while helium implanted

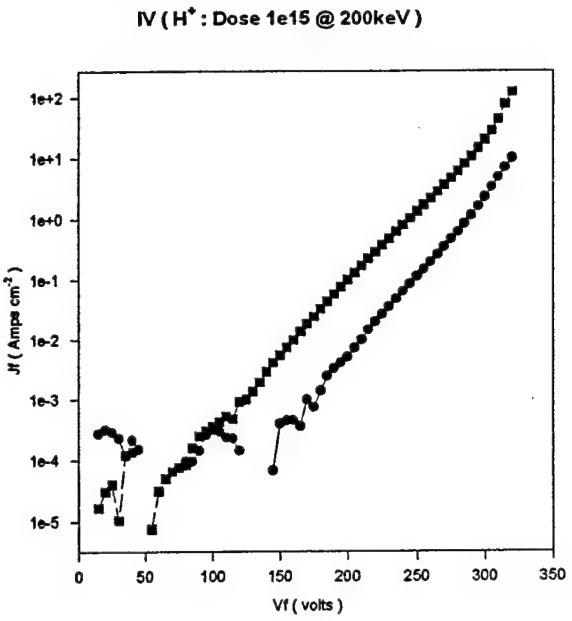


Fig. 11(a)

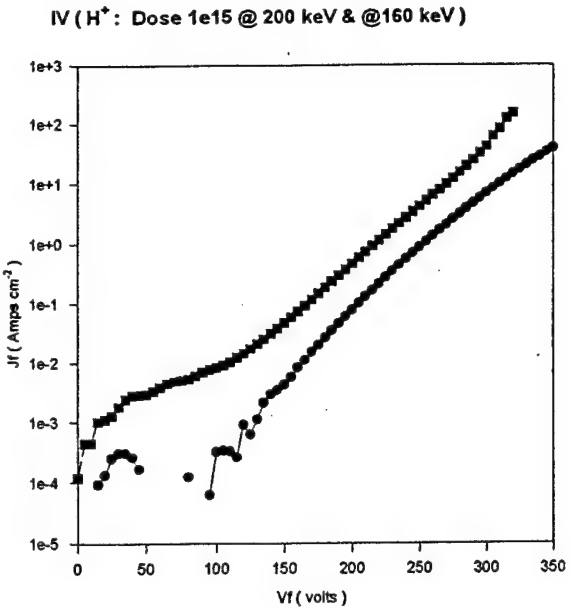


Fig. 11(b)

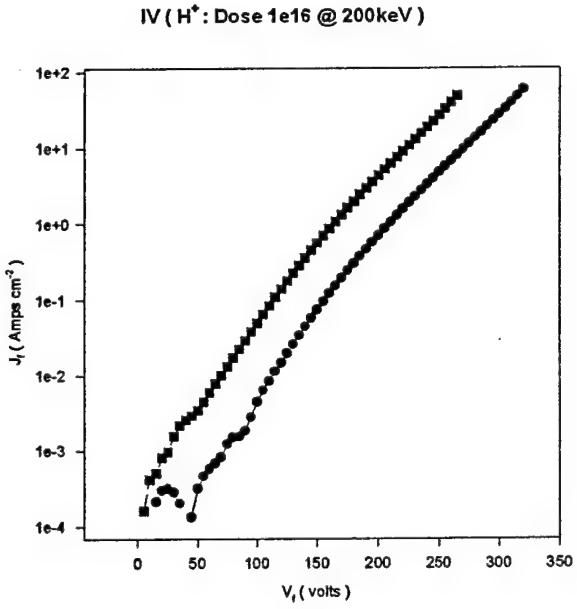


Fig. 11(c)

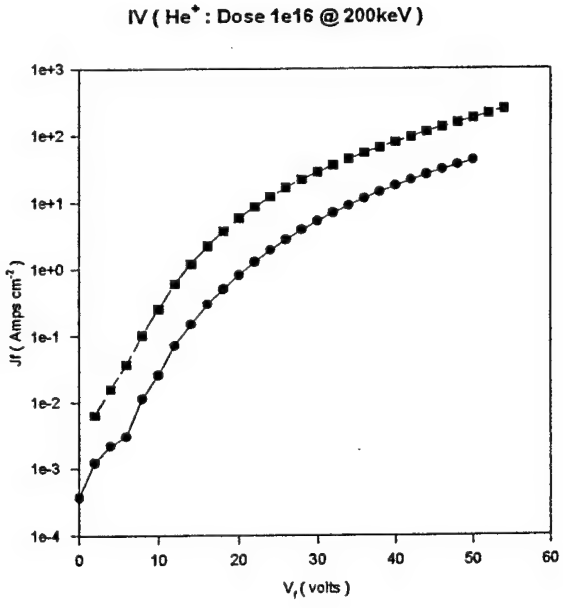


Fig. 11(d)

Fig. 11 (a-d) I-V at room temperature and at 400°K

28V. The low breakdown voltage of the helium implanted layer can be attributed to the possible amorphization of the material. For the fabricated diodes of 100μm and 350μm diameter, it was also found that the characteristics are independent of the area.

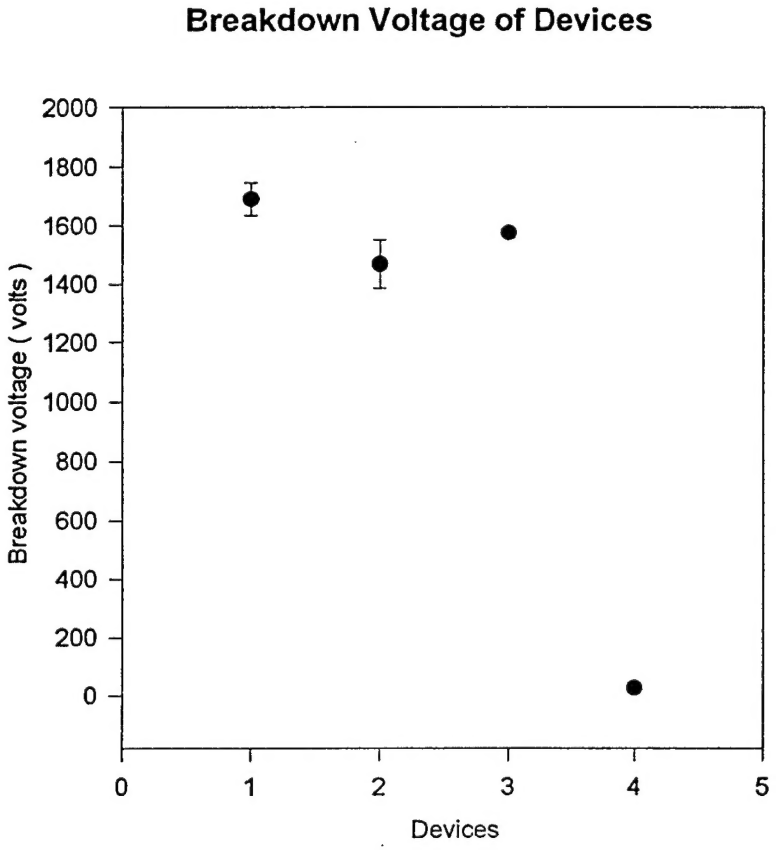


Fig. 12 Breakdown voltage of the devices (1) Low H^+ implanted devices (2) Two low H^+ implanted devices (3) High H^+ implanted devices (4) He^+ implanted devices

B. DLTS measurement

DLTS measurement is most sensitive tool to determine characteristic electrical properties of the deep levels. The measurement is based on the capacitance transient during impurity charge transfer. There are various approaches of doing these measurement[6], but the measurements using DLTFS is considered to have best noise suppression and measuring accuracy. The DLTFS measurement was done on the Schottky diodes using BL8000, 'BIORAD' system. For a material having one or two trap levels, the Arrhenius plot can provide impurity(s)'s, energy level(s) and concentration(s). In the implant many trap levels has been found to be created and evaluation using Arrhenius plot is not possible. So looking at the first sine coefficient of the Fourier transform, 'b1', some predictions can be made regarding the defects levels. coefficient , 'b1', behaves similar to the DLTS signal obtained from a normal boxcar system. In the fig. 13 the 'b1' vs temperature over the wide temperature range is given. It can be concluded from the plots is that the trap levels are created close to the E_C and E_V levels.

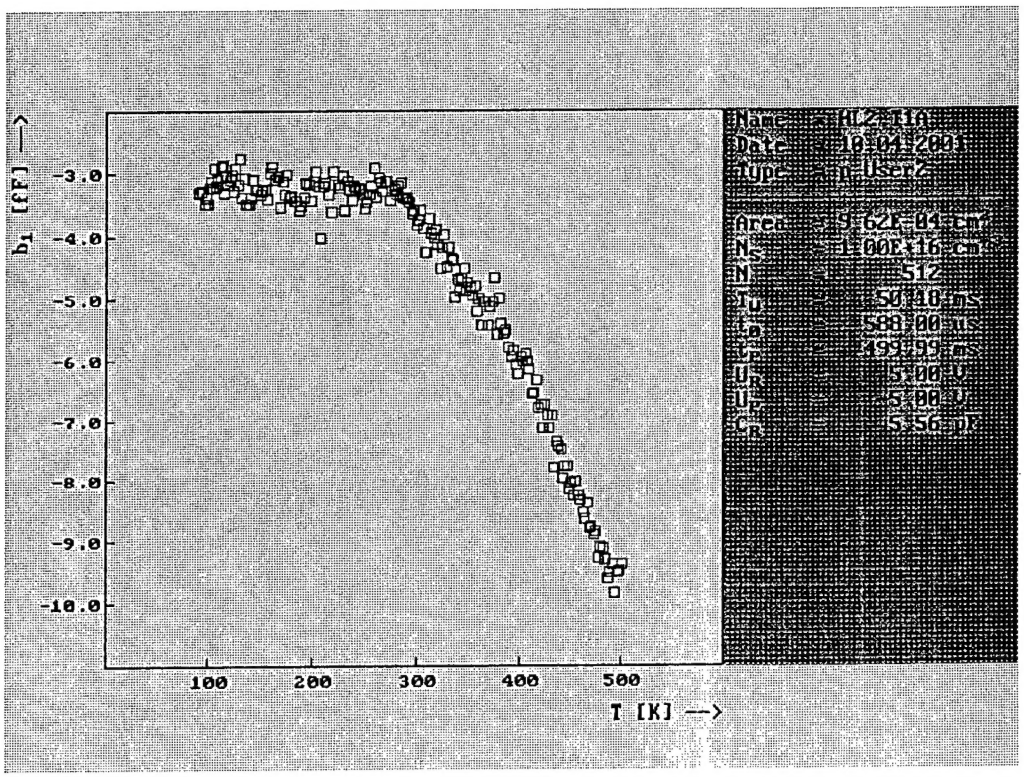


Fig.13 coefficient 'b1' vs temperature for low hydrogen implanted Schottky diode

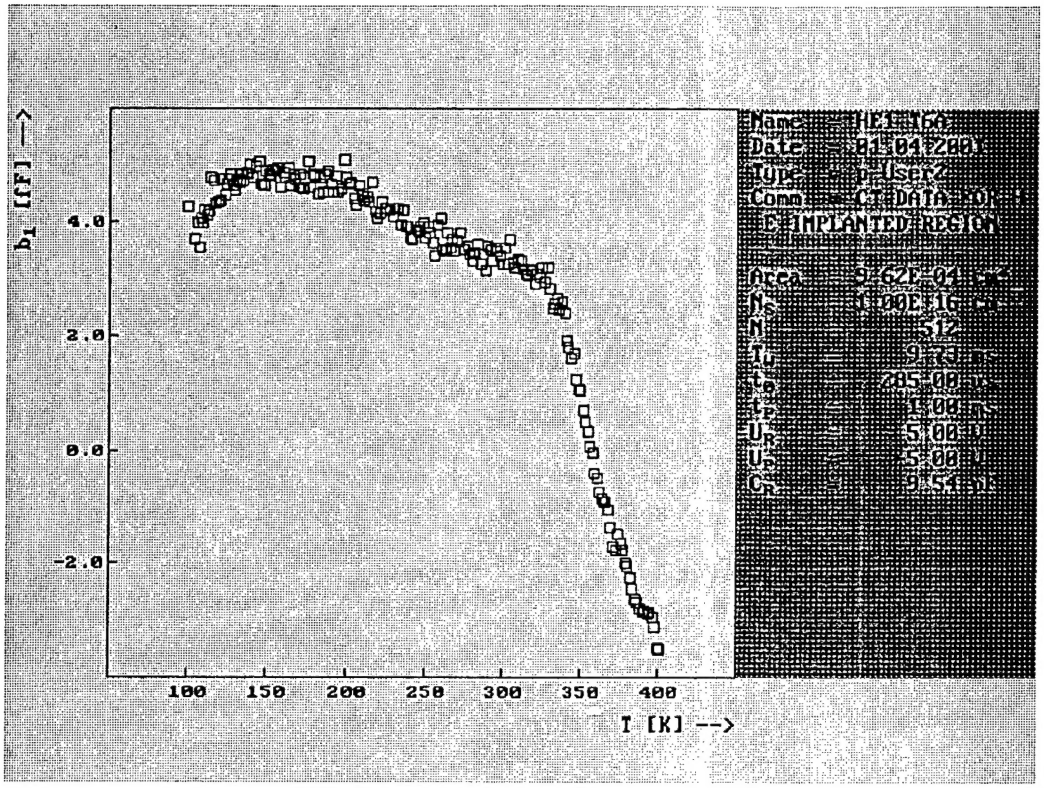


Fig.14 coefficient 'b1' vs temperature for helium implanted Schottky diode

V. Conclusion

In the present work through simulations it has been demonstrated that the vertically isolated MOSFETs can be fabricated on top of the isolation layer provided the layer are deeper than a certain depth. The required depth depends upon the operating voltage of the device. The isolation layer can be formed using hydrogen ion implantation.

Acknowledgment

The authors wish to thank the ONR for supporting this work. The authors also wish to thank TMA for providing simulation software.

References

1. L. Wang et al, " Investigation of damage behavior and isolation effect of n-type 6H-SiC by implantation of oxygen", J. Appl. Phys., vol 33, 2000.
2. B. Aspar et al, " New semiconductor hetero-substrate for high temperature application using the smartcut^{R} technology", The third European conference on High Temperature Electronics, 1999, HITEN99.

3. T. Kimoto et al, " Formation of semi-insulating 6H-SiC layers by vanadium ion implants", Appl. Phys. Lett., vol 69, Aug 1996.
4. R. K. Nadella and M. A. Capano, " High resistance layers in n-type 4H-silicon carbide by Hydrogen ion implantation," Appl. Phys. Lett., vol 70, Feb 1997.
5. R. Raghunathan and B. J. Baliga, " p-type 4H and 6H-SiC High-voltage Schottky barrier diodes," IEEE electron device letters, vol. 19 pp. March 1998.
6. D. K. Schroeder, " Semiconductor material and device characterization," John Wiley and Sons, 1990.